P-Channel Enhancement Mode MOSFET

GENERAL DESCRIPTION

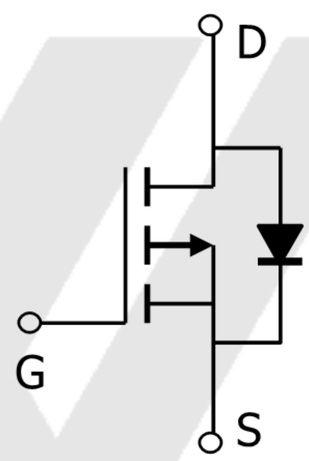
The PW2337 uses advanced trench technology to provide excellent RDS(ON), low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

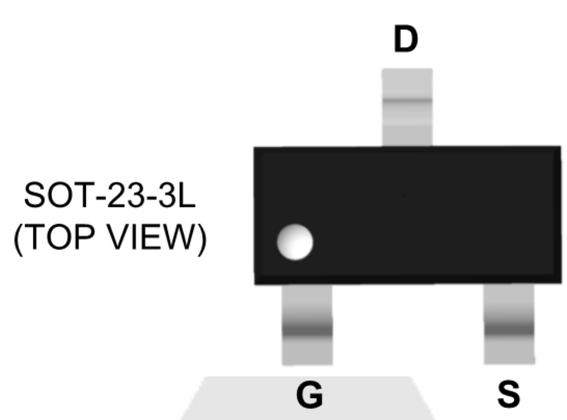
FEATURES

VDS = -100V, ID = -0.9A
RDS(ON) < 650mΩ @ VGS=-10V
Available in a 3-Pin SOT23-3 Package

Application

Battery protection
Load switch
Uninterruptible power suppl





Products

Absolute Maximum Ratings (TA=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current, VGS @ -10V (NOTE1)	I_D@TA=25℃	-0.9	A
	I_D@TA=70℃	-0.7	A
Pulsed Drain Current (NOTE2)	I_{DM}	-1.8	A
Total Power Dissipation (NOTE3)	P_D @TA=25℃	1	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃
Thermal Resistance Junction-Ambient (NOTE1)	$R_{\theta JA}$	125	℃/W
Thermal Resistance Junction-Case (NOTE1)	$R_{\theta JC}$	80	℃/W

Note 1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

Note 2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

Note 3.The power dissipation is limited by 150℃ junction temperature

ELECTRICAL CHARACTERISTICS

(TA = 25°C, unless otherwise noted.)

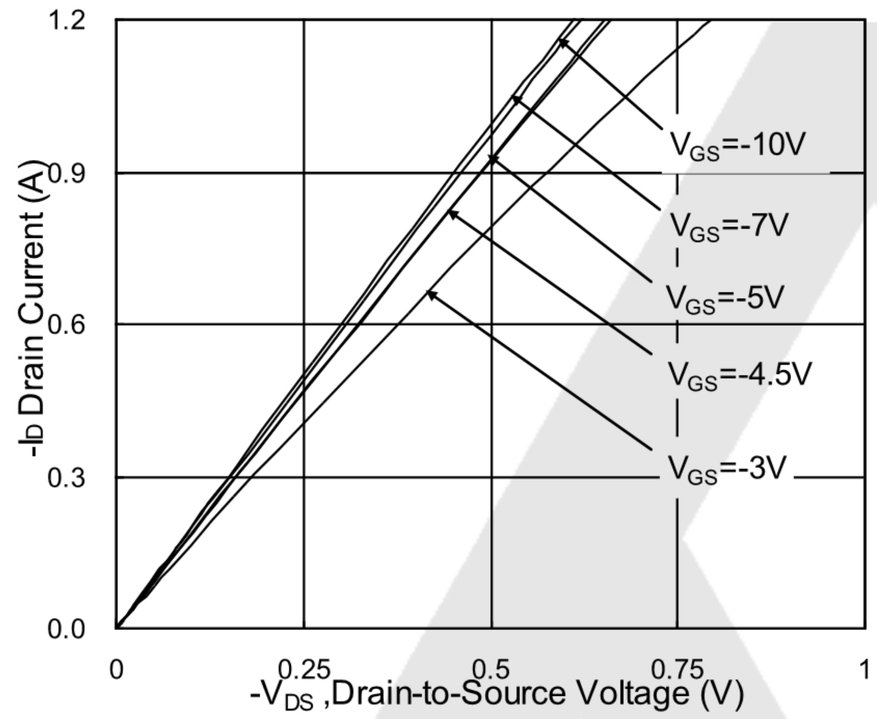
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-100			V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25℃ , I_D=-1mA		-0.063		V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance (NOTE2)	V_{GS}=-10V , I_D=-0.8A		520	650	mΩ
		V_{GS}=-4.5V , I_D=-0.4A		561	699	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.0	-1.5	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient			4.5		mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-80V , V_{GS}=0V , T_J=25℃			-10	uA
		V_{DS}=-80V , V_{GS}=0V , T_J=55℃			-100	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V			±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-0.8A		3		S
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-15, V_{GS}=-4.5V , I_D=-0.5		4.5		nC
Q_{gs}	Gate-Source Charge			1.14		nC
Q_{gd}	Gate-Drain Charge			1.5		nC
$T_{d(on)}$	Turn-On Delay Time	V_{DS}=-50V, V_{GS}=-10V R_G=3.3Ω, I_D=-0.5A		13.6		ns
T_r	Rise Time			6.8		ns
$T_{d(off)}$	Turn-Off Delay Time			34		ns
T_f	Fall Time			3		ns
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz		553		pF
C_{oss}	Output Capacitance			29		pF
C_{rss}	Reverse Transfer Capacitance			20		pF
I_S	Continuous Source Current(NOTE1, 3)	V_G=V_D=0V , Force Current			-0.9	A
I_{SM}	Pulsed Source Current(NOTE2, 3)				-1.8	A
V_{SD}	Diode Forward Voltage (NOTE2)	V_{GS}=0V , I_S=-1A , T_J=25℃			-1.2	V

Note 1.The data tested by surface mounted on a 1 $inch^2$ FR-4 board with 2OZ copper.

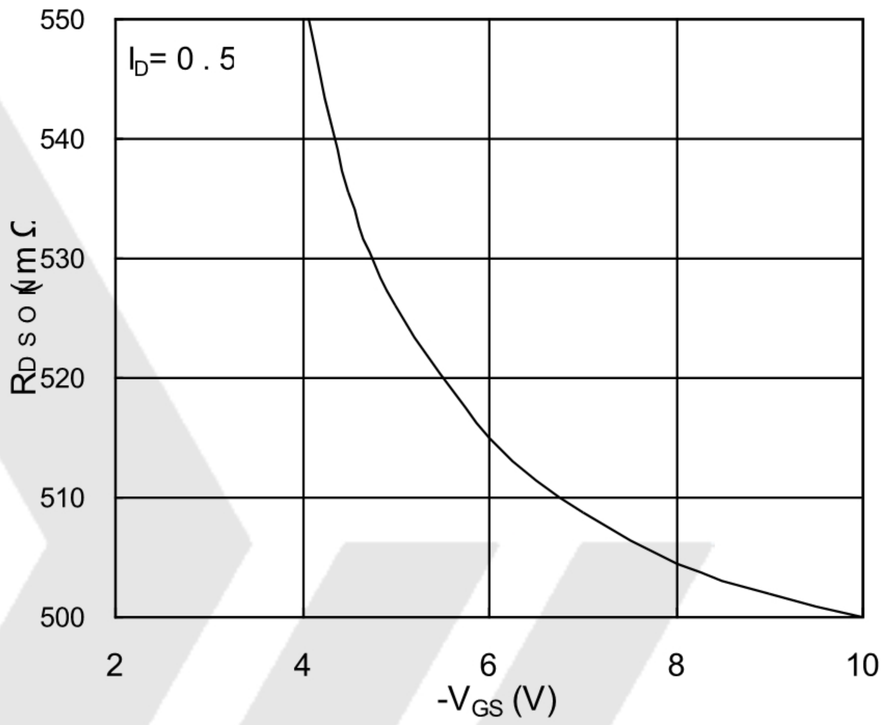
Note 2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

Note 3.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation

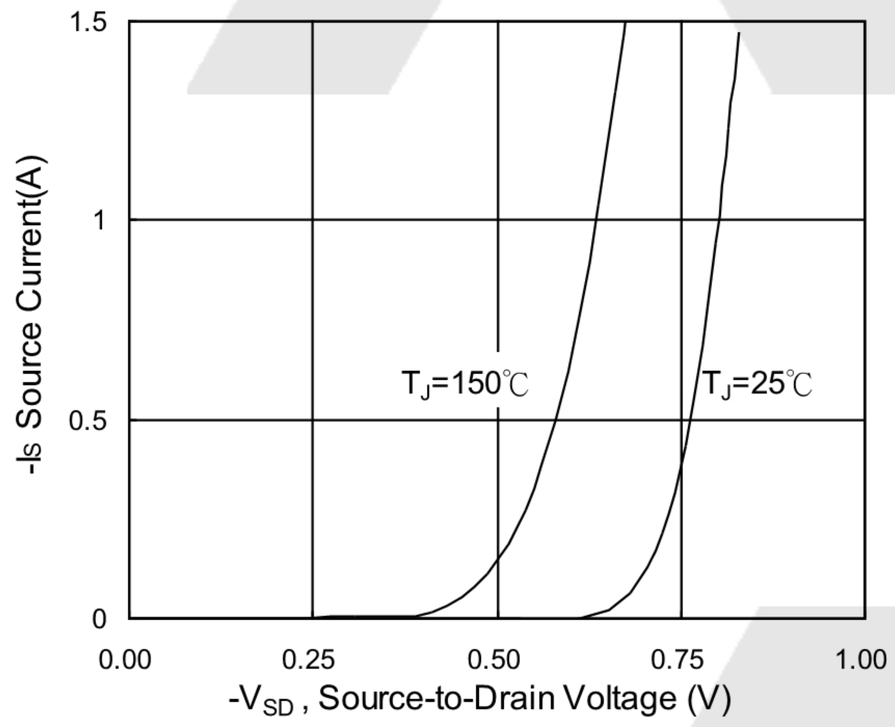
Thermal Characteristics



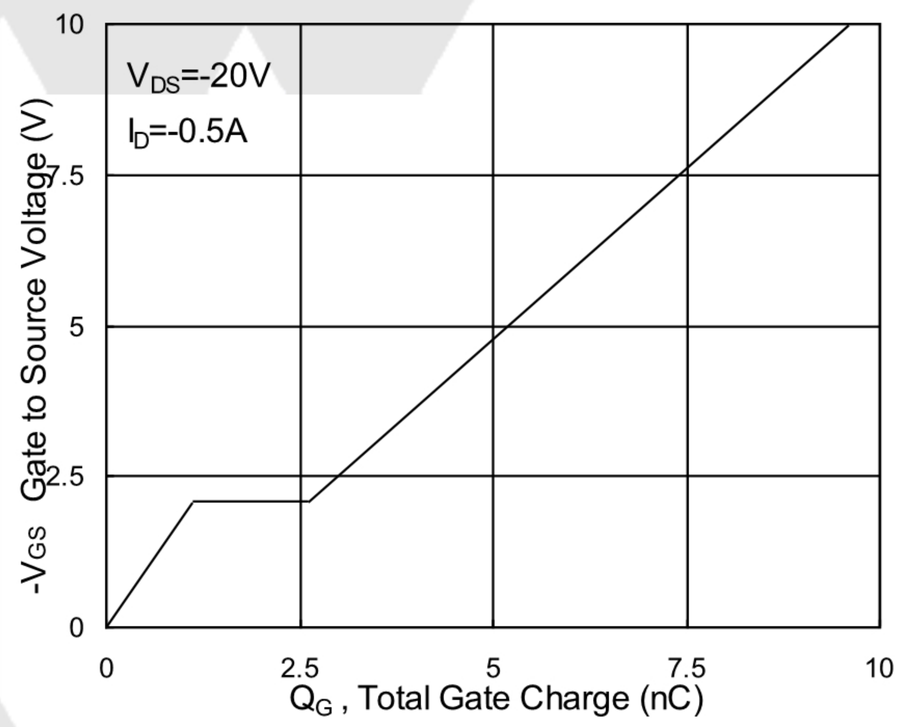
Typical Output Characteristics



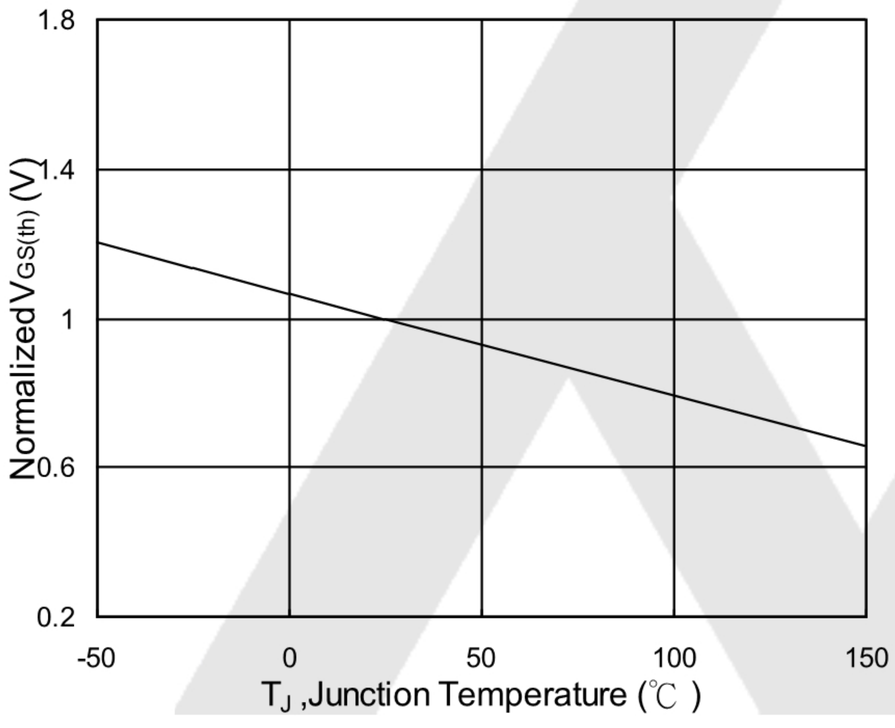
On-Resistance v.s Gate-Source



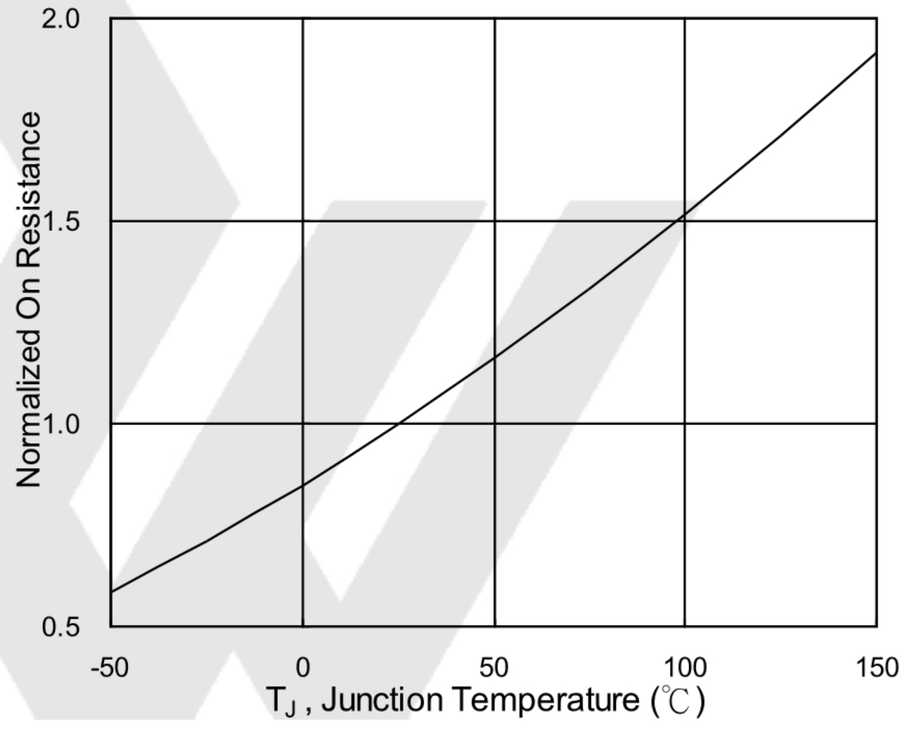
Forward Characteristics Of Reverse



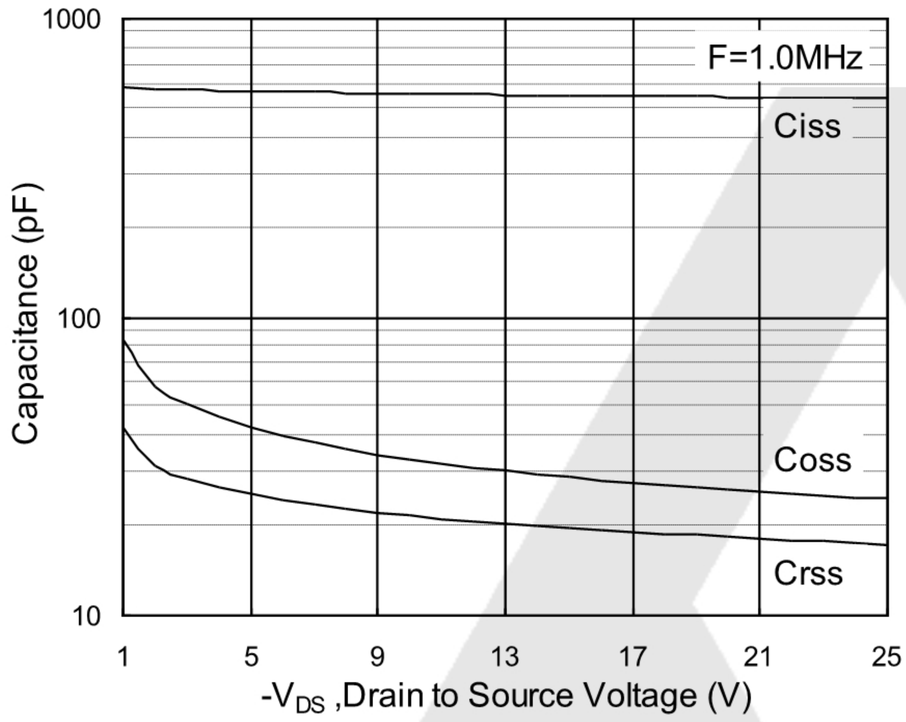
Gate-Charge Characteristics



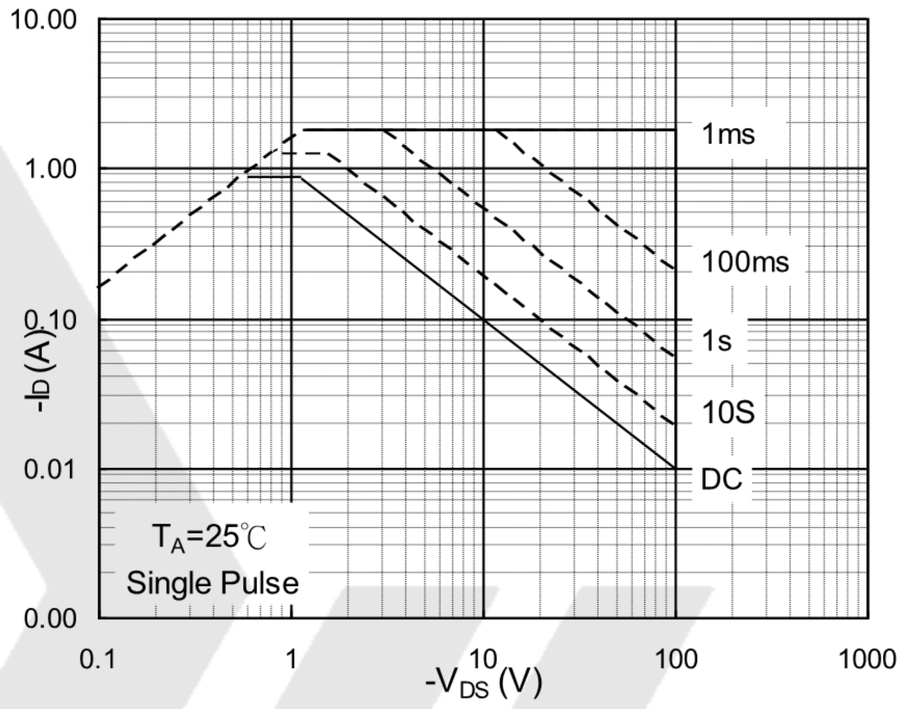
Normalized VGS(th) v.s TJ



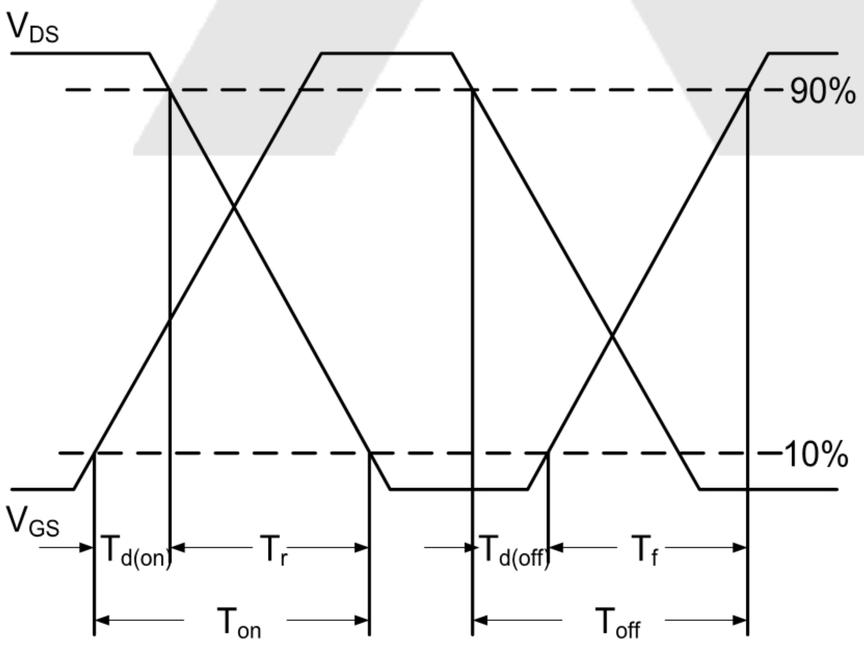
Normalized RDSON v.s TJ



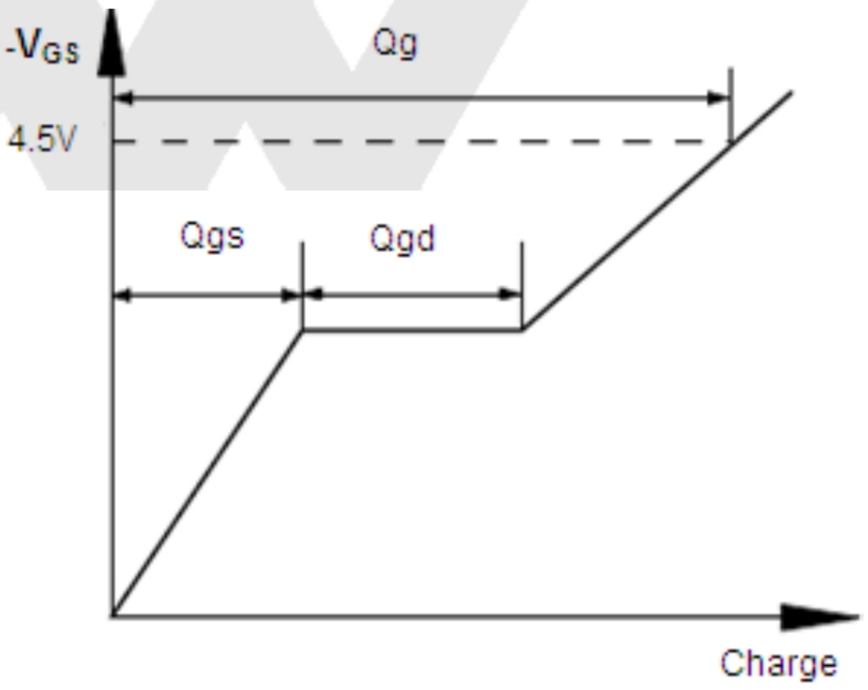
Capacitance



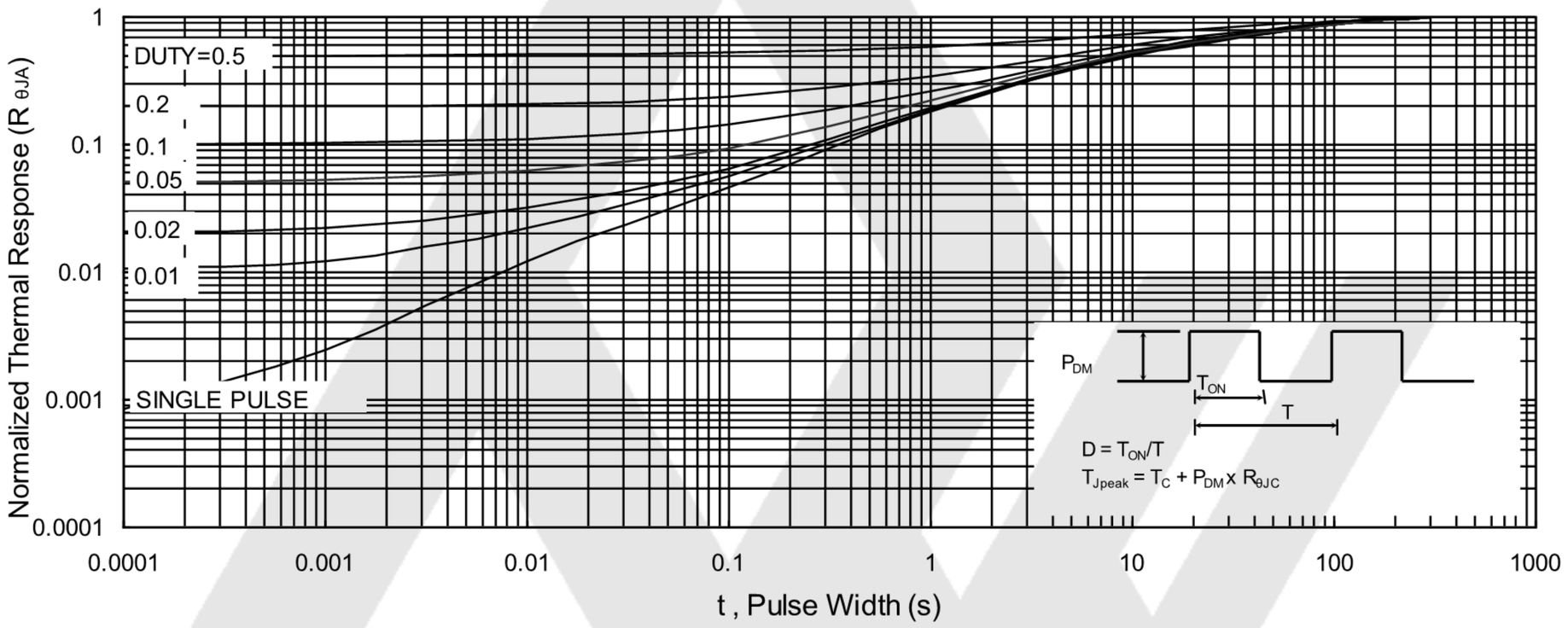
Safe Operating Area



Switching time waveform



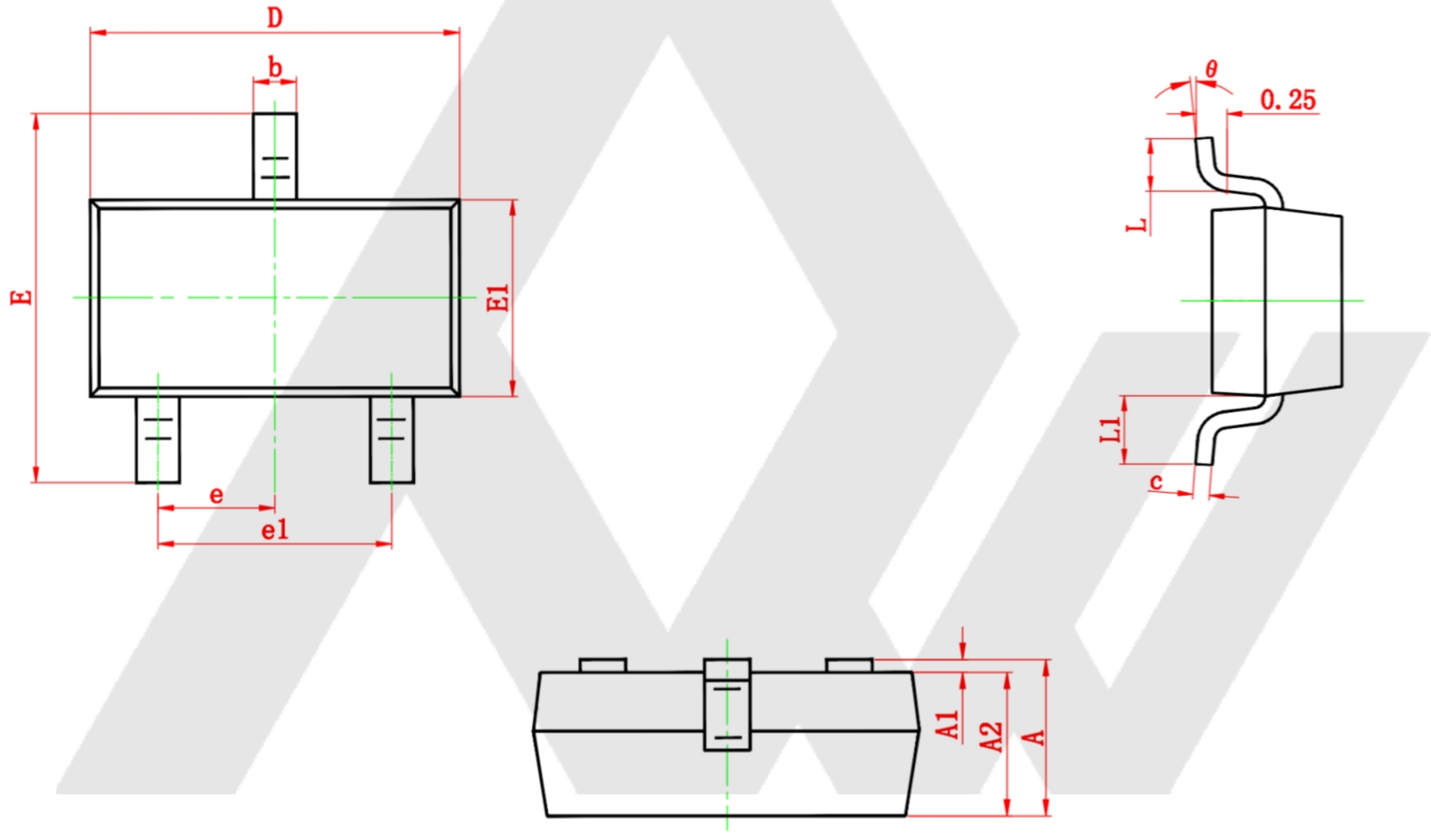
Gate Charge waveform



Normalized Maximum Transient Thermal Impedance

PACKAGE DESCRIPTION

SOT23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	2.250	2.550	0.089	0.100
E1	1.200	1.400	0.047	0.055
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.300	0.500	0.012	0.020
L1	0.550 REF.		0.022 REF.	
θ	0°	8°	0°	8°

Notes

1. All dimensions are in millimeters.
2. Tolerance ±0.10mm (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

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