100KHz to 1.1MHz，5A，3.8V-36V Input，
synchronous Step Down Regulator

DESCRIPTION

The PW2458 is 5A synchronous buck converters with wide input voltage, ranging from 3.8V to 36V, which integrates a 45mΩ high-side MOSFET and a 20mΩ low-side MOSFET. The PW2458, adopting the peak current mode control, supports the Pulse Skipping Modulation (PSM) with typical 25uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

The PW2458 features programmable switching frequency from 100 kHz to 1.1 MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size. The converter supports external clock synchronization with a frequency band from 100kHz to 1.1MHz. The PW2458 allows power conversion from high input voltage to low output voltage with a minimum 100ns on-time of high-side MOSFET.

The PW2458 is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The PW2458 features Frequency Spread Spectrum FSS with ±6% jittering span of the 500kHz switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI. The PW2458 offers cycle-by-cycle current limit and hiccup over current protection, thermal shutdown protection, output over-voltage protection and input voltage under-voltage protection. The device is available in an 8-pin thermally enhanced SOP8-EP package.

FEATURES

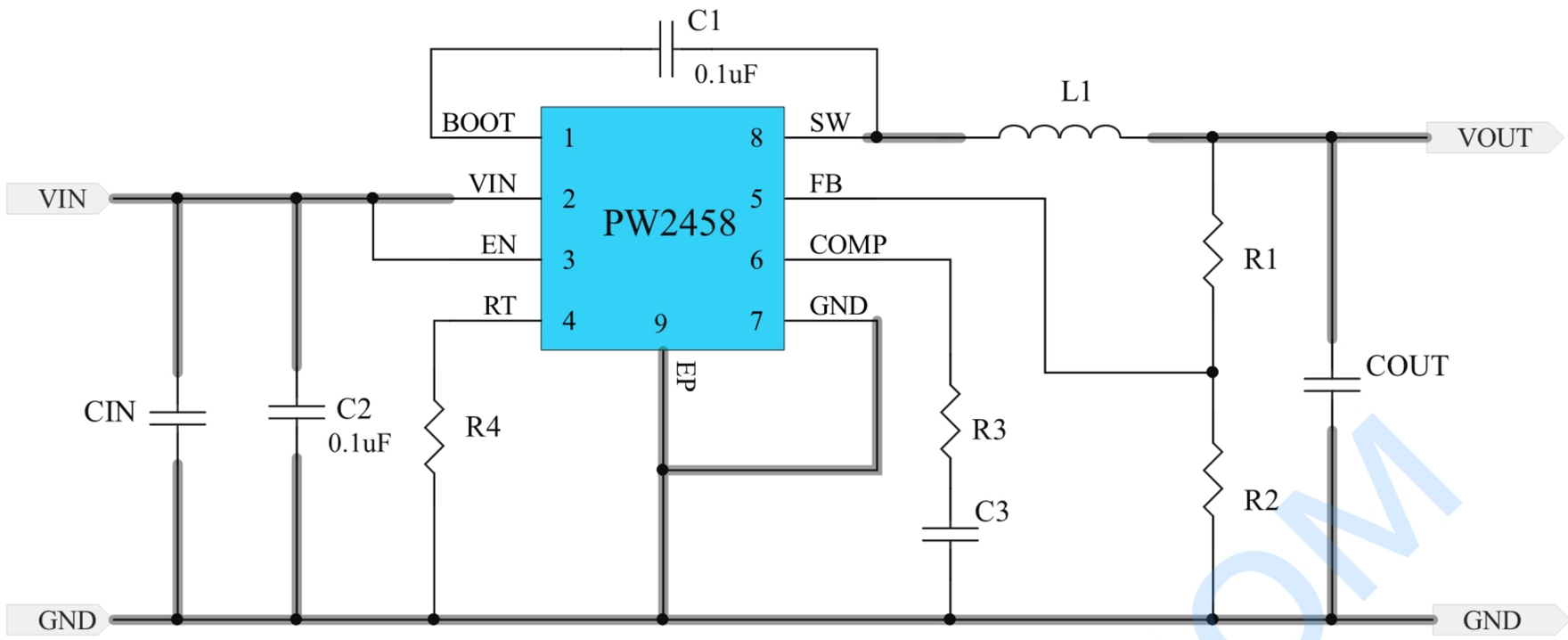
- Wide Input Range: 3.8V-36V
- Up to 5A Continuous Output Current
- 0.8V ±1% Feedback Reference Voltage
- Integrated 45mΩ High-Side and 20mΩ Low-Side Power MOSFETs
- Pulse Skipping Mode (PSM) with 25uA Quiescent Current in Sleep Mode
- 100ns Minimum On-time
- 4ms Internal Soft-start Time
- Adjustable Frequency 100KHz to 1.1MHz
- External Clock Synchronization
- Frequency Spread Spectrum (FSS) Modulation for EMI Reduction
- Precision Enable Threshold for Programmable Input Voltage Under-voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Low Dropout Mode Operation
- Derivable Inverting Voltage Regulator
- Over-voltage and Over-Temperature Protection
- Available in an SOP8-EP Package

APPLICATIONS

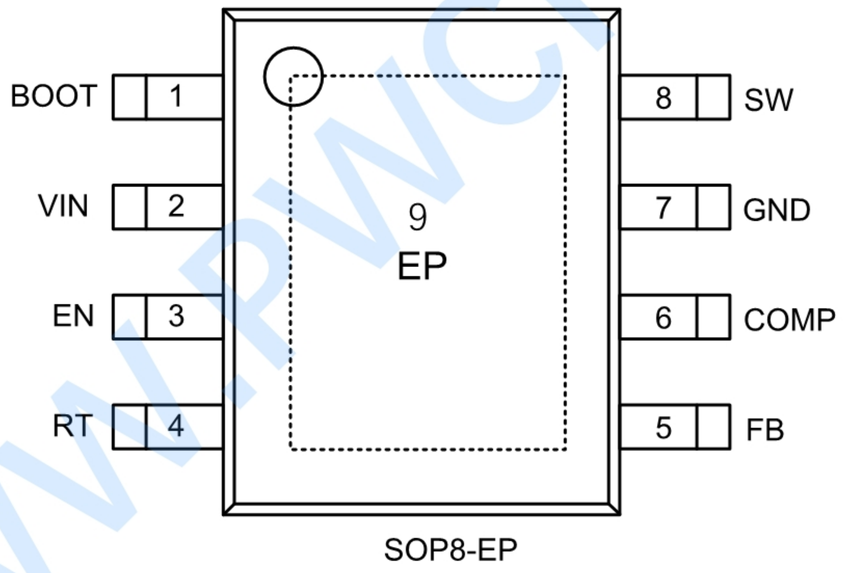
- Battery Pack Powered System - Cordless Power Tools,
- Cigarette Lighter Adapters, Chargers
- LCD Display
- USB Type-C Power Delivery, USB Charging
- Automotive System

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TYPICAL APPLICATION



PIN CONFIGURATION



SOP8-EP

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
BOOT	1	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
VIN	2	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
EN	3	Enable pin to the regulator with internal pull-up current source. Pull below 1.1V to disable the converter. Float or connect to VIN to enable the converter. The tap of resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.

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RT	4	Set the 20internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT pin. The internal oscillator synchronizes to the external clock frequency with PLL. If detected clocking edges stops, the operation mode automatically returns to resistor programmed frequency.
FB	5	Inverting input of the trans-conductance error amplifier. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 0.8V typical.
COMP	6	Error amplifier output. Connect to frequency loop compensation network.
GND	7	Ground.
SW	8	Regulator switching output. Connect SW to an external power inductor.
EP	9	Heat dissipation path of die. Electrically connect ground plane on PCB for proper operation and optimized thermal performance. ion to GND pin. Must be connected to.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise (note1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	38	V
BOOT	-0.3	44	V
SW	-1	38	V
BOOT-SW	-0.3	6	V
COMP, FB, RT	-0.3	6	V
Operating junction temperature TJ (note2)	-40	150	°C
Storage temperature TSTG	-65	150	°C

NOTE:

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
VIN	Input voltage range	3.8	36	V
VOUT	Output voltage range	0.8	36	V
TJ	Operating junction temperature	-40	125	°C
HBM	Human Body Model, per ANSI-JEDEC-JS-001-2014 specification, all pins(Note 1)	-2	+2	kV
CDM	Charged Device Model, per ANSI-JEDEC-JS-002- 2014 specification, all pins(Note 2)	-0.5	+0.5	kV
RθJA	Junction to ambient thermal resistance(Note 3)	42		°C/W
RθJC	Junction to case thermal resistance(Note 3)	45.8		°C/W

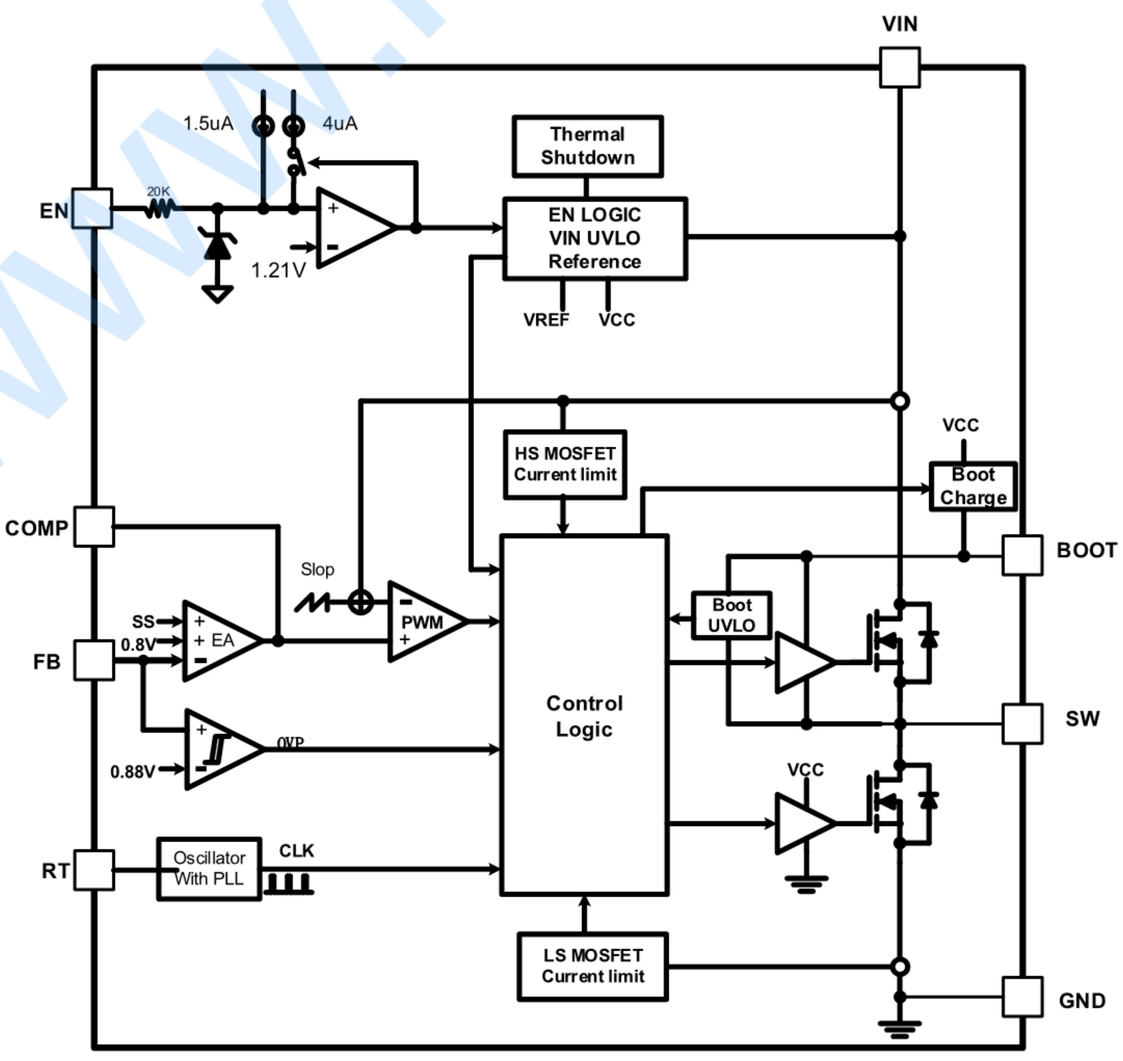
Note:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

(3) PWchip provides RθJA and RθJC numbers only as reference to estimate junction temperatures of the devices. RθJA and RθJC are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the PW2458 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the PW2458. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual RθJA and RθJC

FUNCTIONAL BLOCK DIAGRAM



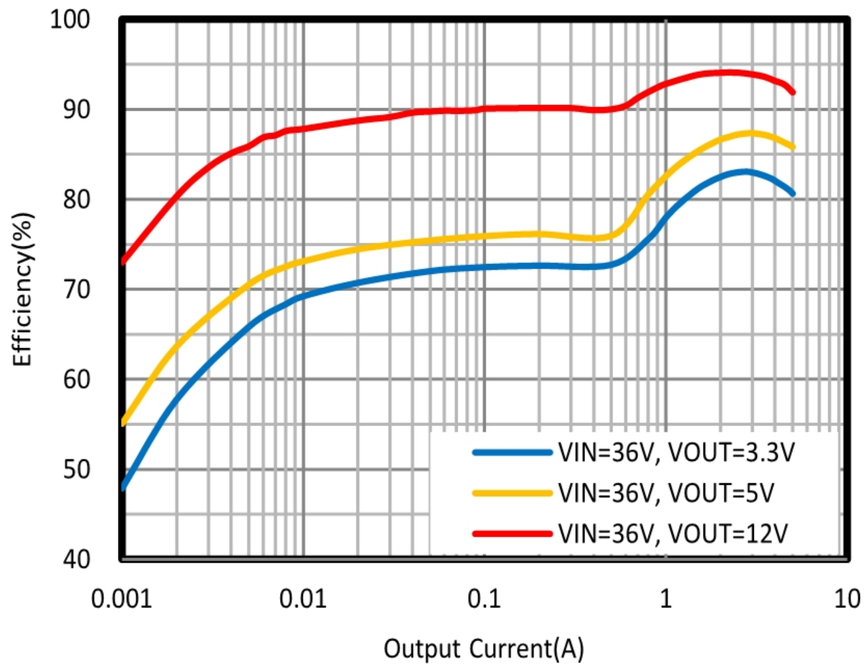
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ELECTRICAL CHARACTERISTICS V_{IN}=24V, T_J=-40°C~125°C, typical value is tested under 25°C.

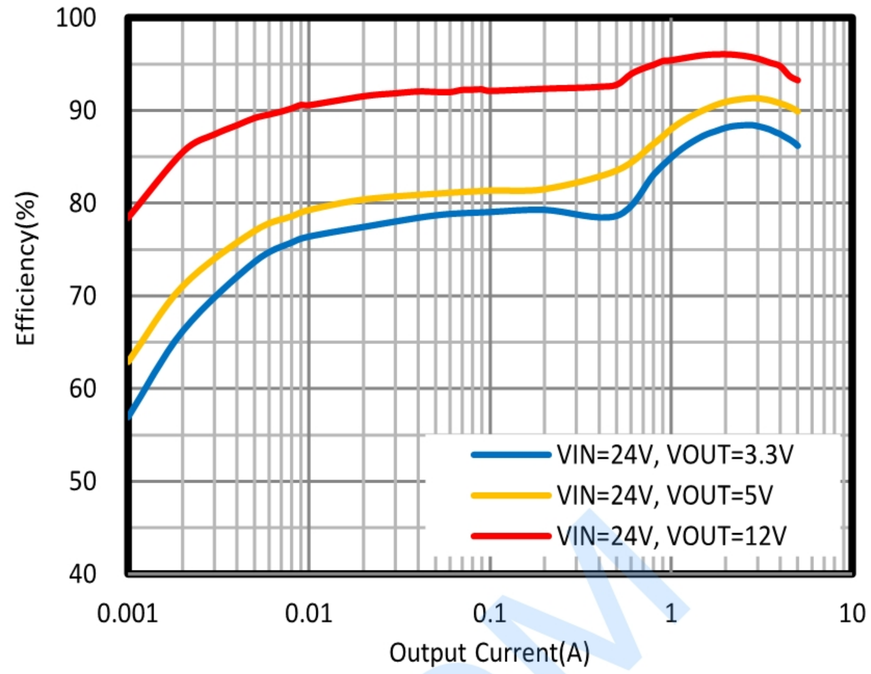
SYMBOL	PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
VIN	Operating input voltage			3.8		36	V
VIN_UVLO	Input UVLO Threshold		VIN rising		3.5	3.7	V
	Hysteresis				400		mV
ISHDN	Shutdown current from VIN pin		EN=0, no load		1	3	μA
IQ	Quiescent current from VIN pin		EN floating,no load, non switching, BOOT-SW=5V		25		μA
RDSON_H	High-side MOSFET on-resistance		VBOOT-VSW=5V		45		mΩ
RDSON_L	Low-side MOSFET on-resistance				20		mΩ
VREF	Reference voltage of FB			0.792	0.8	0.808	V
GEA	Error amplifier trans-conductance	VCOMP=1V	-2μA<ICOMP<2μA,		300		μS
ICOMP_SRC	EA maximum source current		VFB=VREF-100mV,		30		μA
ICOMP_SNK	EA maximum sink current		VFB=VREF+100mV,		30		μA
VCOMP_H	COMP high clamp				3		V
VCOMP_L	COMP low clamp				0.4		V
ILIM_HS	High-side power MOSFET peak current limit threshold			6.8	8	9.2	A
ILIM_LSSRC	Low-side power MOSFET souring current limit threshold				9		A
THIC_W	Over current protection hiccup wait time				512		cycles
THIC_R	Over current protection hiccup restart time				8192		cycles
VEN_H	Enable high threshold				1.18	1.25	V
VEN_L	Enable low threshold			1.03	1.1		V
IEN_L	Enable pin pull-up current		EN=1V	1	1.5	2	μA
IEN_H	Enable pin pull-up current		EN=1.5V		5.5		uA
Tss	Internal soft start time				4		ms
FRANGE_RT	Frequency range using RT mode			100		100	kHz
FSW	Switching frequency		RRT=200 kΩ(1%)	450	500	550	kHz
FRANGE_CLK	Frequency range using CLK mode			100		1100	kHz
FJITTER	Frequency spread spectrum in percentage of Fsw				±6		%
tON_MIN	Minimum on-time		VIN=24V		100		ns
VOVP	Feedback overvoltage with respect to reference voltage		VFB/VREF rising		110		%
			VFB/VREF falling		105		%
VBOOTUV	BOOT-SW UVLO threshold		BOOT-SW falling		2.36		V
			Hysteresis		300		mV
TSD	Thermal shutdown threshold		TJ rising Hysteresis		170		°C
					25		°C

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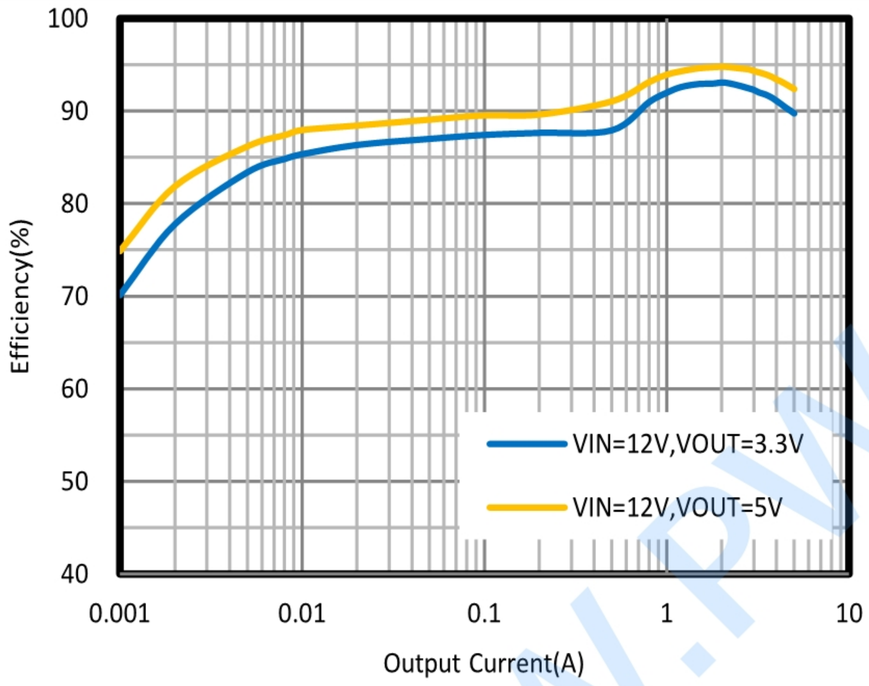
TYPICAL CHARACTERISTICS



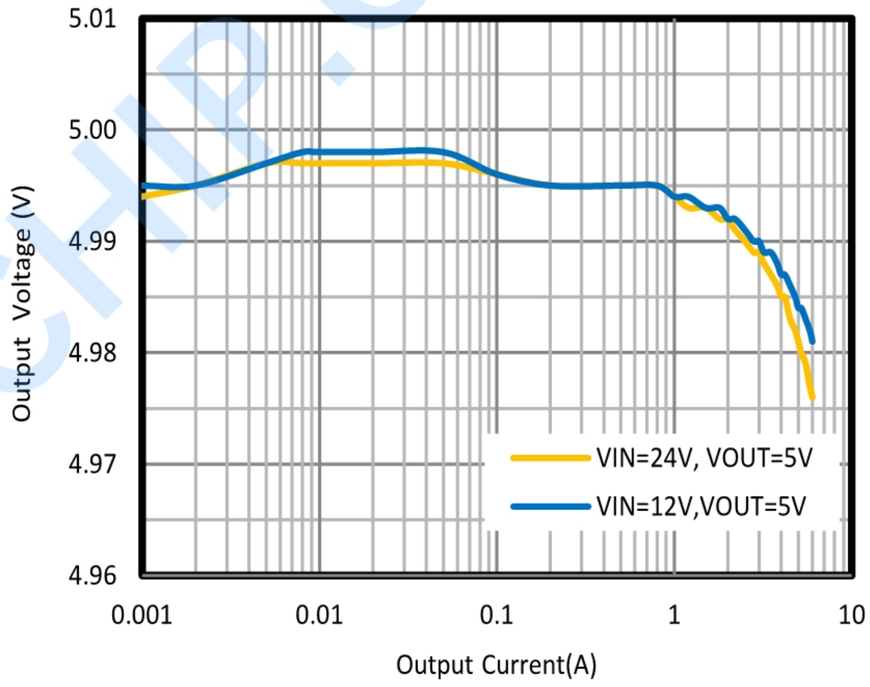
Efficiency vs Load Current, Vin=36V



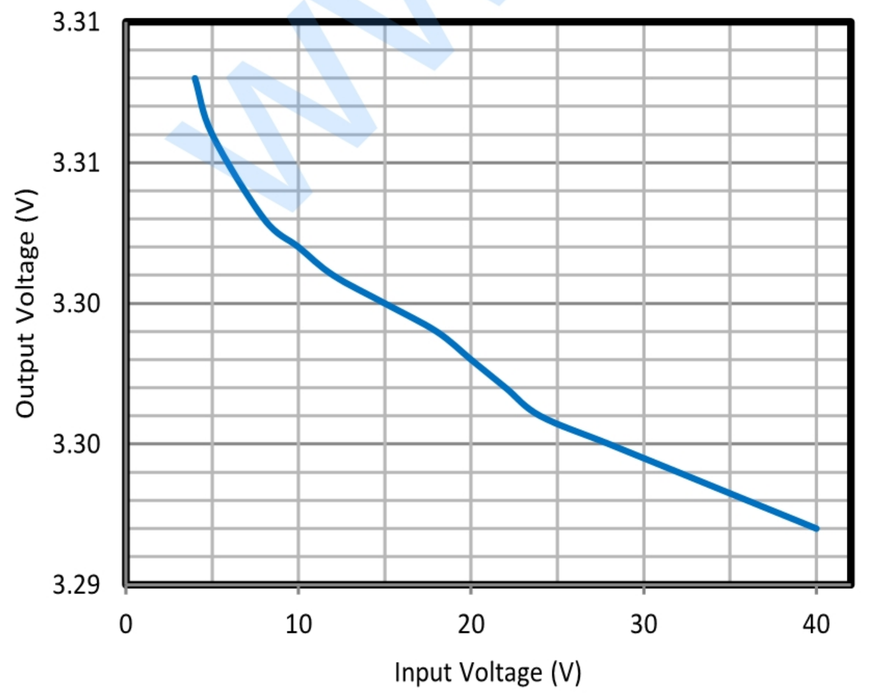
Efficiency vs Load Current, Vin=24V



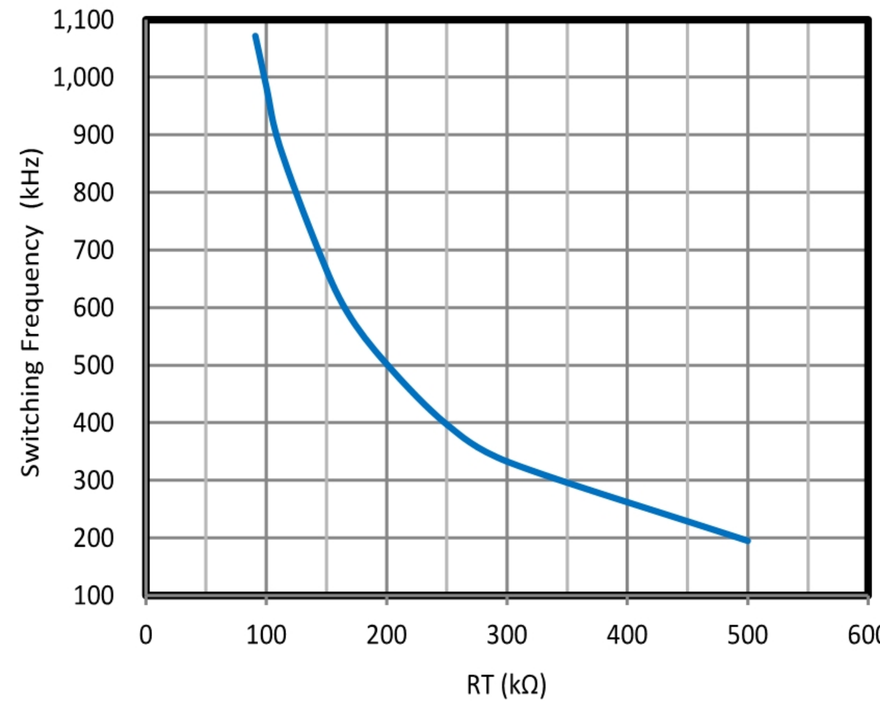
Efficiency vs Load Current, Vin=12V



Load Regulation (Vout=5V)

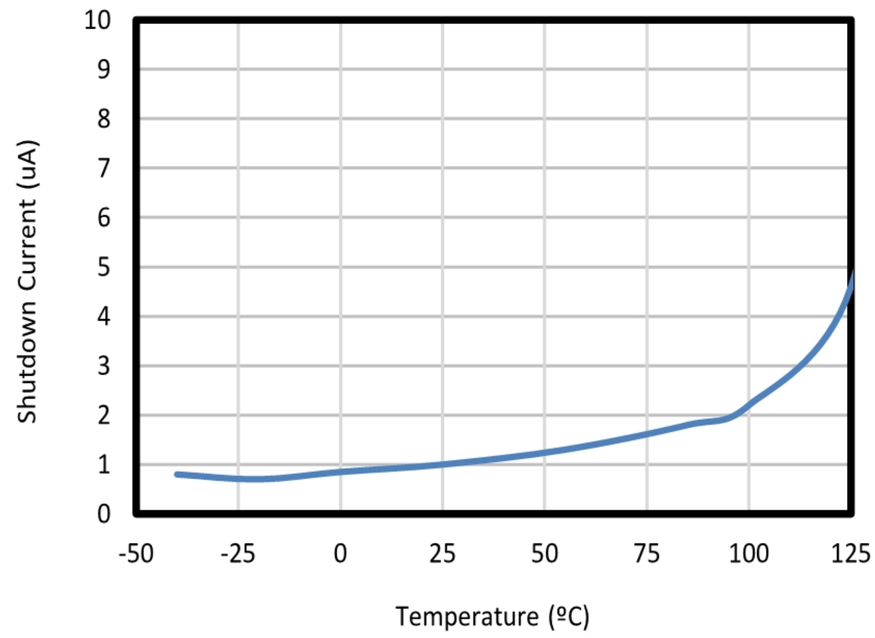


Line Regulation (Iout=5A)

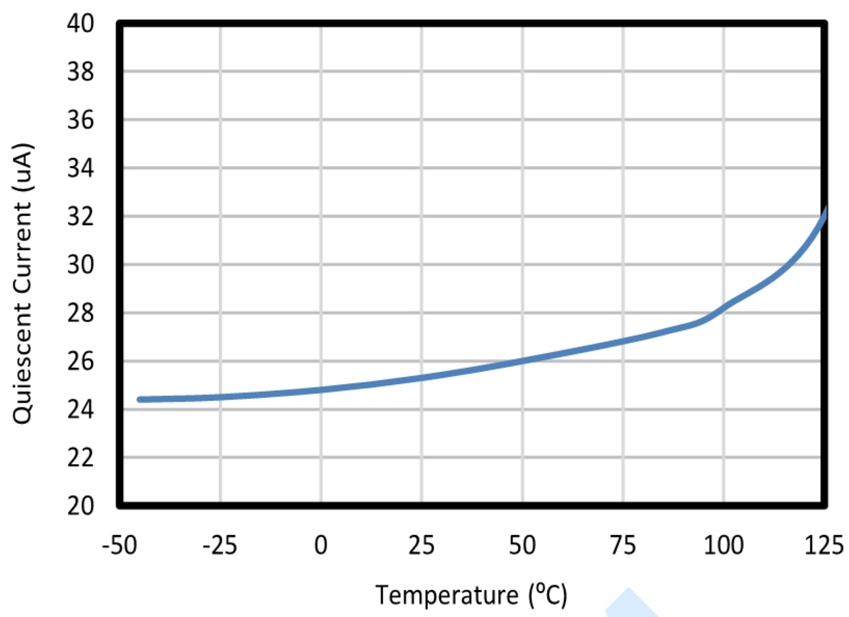


Clock Frequency vs RT Resistor

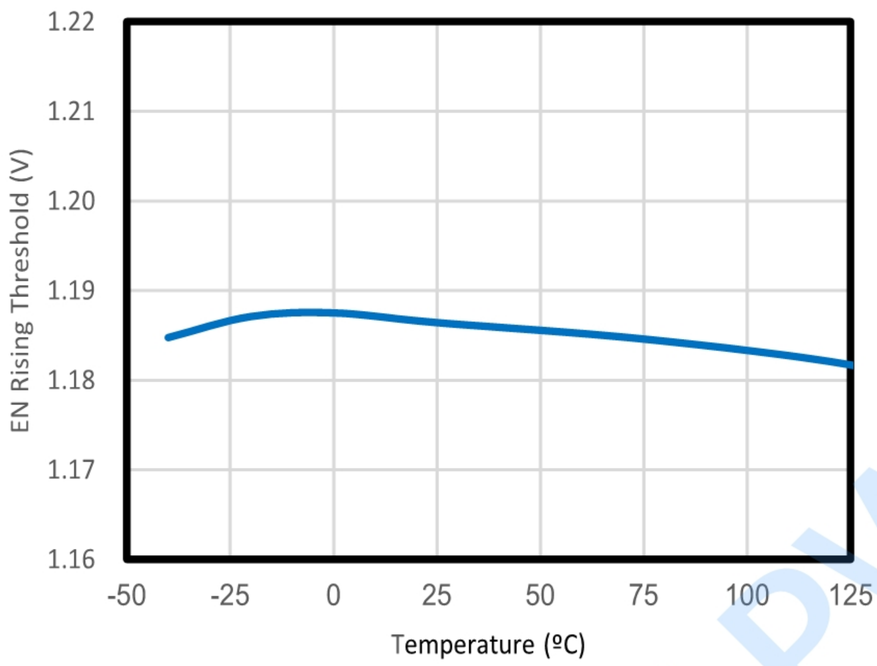
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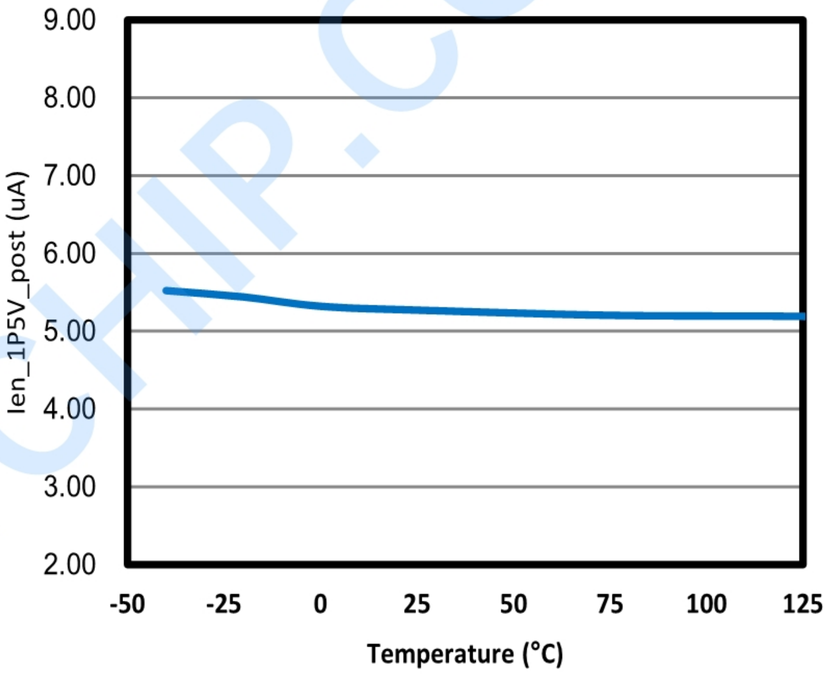
Shutdown Current vs Temperature



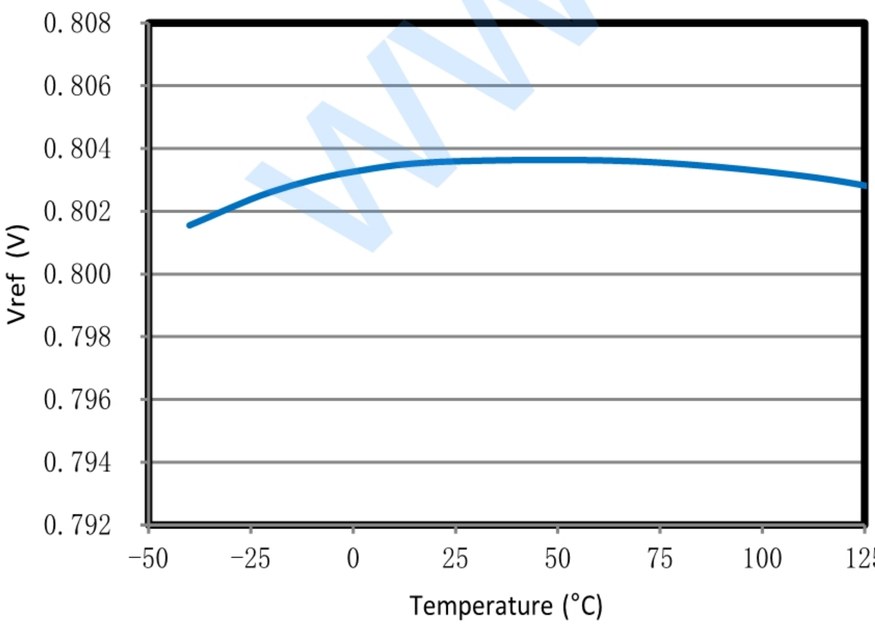
Quiescent Current vs Temperature



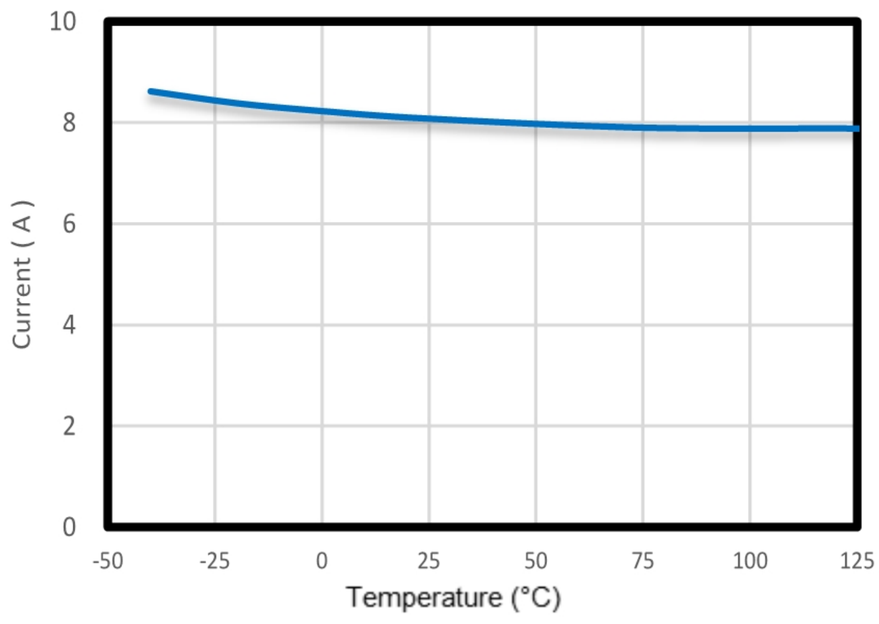
EN Threshold vs Temperature



EN Pull-up Current vs Temperature



Reference Voltage vs Temperature



Peak Current Limit vs Temperature

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OPERATION

Overview

The PW2458 is a 3.8V-36V input, 5A output, EMI friendly synchronous buck converter with built-in 45mΩ Rdson high-side and 20mΩ Rdson low-side power MOSFETs. It implements constant frequency peak current mode control to regulate output voltage, providing excellent line and load transient response and simplifying the external frequency compensation design.

The switching frequency is programmable from 100kHz to 1.1MHz with two setting modes, resistor setting frequency mode and the clock synchronization mode, to optimizes either the power efficiency or the external components' sizes. The PW2458 features an internal 4ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The seamless mode-transition between PWM mode and PSM mode operations ensure high efficiency over wide load current range. The quiescent current is typically 25uA under no load or sleep mode condition to achieve high efficiency at light load.

The PW2458 has a default input start-up voltage of 3.5V with 400mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly starts up the device automatically.

The PW2458 implements the Frequency Spread Spectrum FSS modulation spreading of ±6% centered selected switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time. The PW2458 full protection features include the input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

Peak Current Mode Control

The PW2458 employs fixed frequency peak current mode control. An internal clock initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the highside MOSFET turns off. The synchronous low-side MOSFET Q2 turns on till the next clock cycle begins or the inductor current falls to zero.

The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent subharmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The PW2458 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, an increment in the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold (400mV typically), device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage, and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse. After several switching cycles with typical 1A peak inductor current, COMP voltage drops and is clamped again and pulse skipping mode repeats if the output continues light loaded.

This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 25uA during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

The PW2458 is enabled when the VIN pin voltage rises about 3.5V and the EN pin voltage exceeds the enable threshold of 1.18V. The device is disabled when the VIN pin voltage falls below 3.1V or when the EN pin voltage is below 1.1V. An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin floats. EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

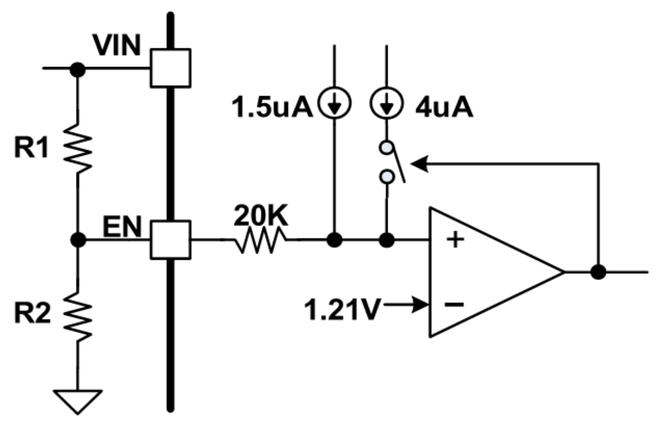
For a higher system UVLO threshold, connect an external resistor divider (R5 and R6) shown from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

$$V_{rise} = 1.18 * \left(1 + \frac{R1}{R2}\right) - 1.5uA * R1 \quad (1)$$

$$V_{fall} = 1.1 * \left(1 + \frac{R1}{R2}\right) - 5.5uA * R1 \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO



System UVLO by enable divide

Output Voltage

The PW2458 regulates the internal reference voltage at 0.8V with ±1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers.To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$\boldsymbol{Vout = \left(\frac{R1}{R2} + 1\right) * Vref \ .(Vref = 0.8V\ (Typ))}$$

Internal Soft-Start

The PW2458 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.8V reference voltage in 4ms. If the EN pin is pulled below 1.1V, switching stops and the internal soft-start resets.The soft-start also resets during shutdown due to thermal overloading.

Switching Frequency and Clock Synchronization

The switching frequency of the PW2458 is set by placing a resistor between RT pin and the ground, or synchronizing to an external clock.

In resistor setting frequency mode, a resistor placed between RT pin to the ground sets the switching frequency over a wide range from 100KHz to 1.1MHz. The RT pin voltage is typical 0.5V. RT pin is not allowed to be left floating or shorted to the ground. Use Equation 4 or the plot. to determine the resistance for a switching frequency needed.

$$\mathrm{R4}\,(\boldsymbol{K\Omega}) = \frac{\mathbf{100000}}{\boldsymbol{Fsw\ \ (KHZ)}}$$

In clock synchronization mode, the switching frequency synchronizes to an external clock applied to RT pin.The synchronization frequency range is from 100KHz to 1.1MHz and the rising edge of the SW synchronizes to the falling edge of the external clock at RT pin with typical 66ns time delay. A square wave clock signal to RT pin must have high level no lower than 2V, low level no higher than 0.4V, and pulse width larger than 80ns.

In applications where both resistor setting frequency mode and clock synchronization mode are needed, the device can be configured as shown . Before an external clock is present, the device works in resistor setting frequency mode. When an external clock presents, the device automatically transitions from resistor setting mode to external clock synchronization mode. An internal phase locked loop PLL locks internal clock frequency onto the external clock within typical 85us. The converter transitions from the clock synchronization mode to the resistor setting frequency mode when the external clock disappears.

Frequency Spread Spectrum

To reduce EMI, the PW2458 implements Frequency Spread Spectrum (FSS). The FSS circuitry shifts the switching frequency of the regulator periodically within a certain frequency range around the programmed switching frequency. The jittering span is ±6% of the switching frequency with 1/512 swing frequency. This frequency dithering function is effective for both frequency programmed by resistor placed at RT pin and an external clock synchronization application.

Bootstrap Voltage Regulator and Low Drop-out Operation

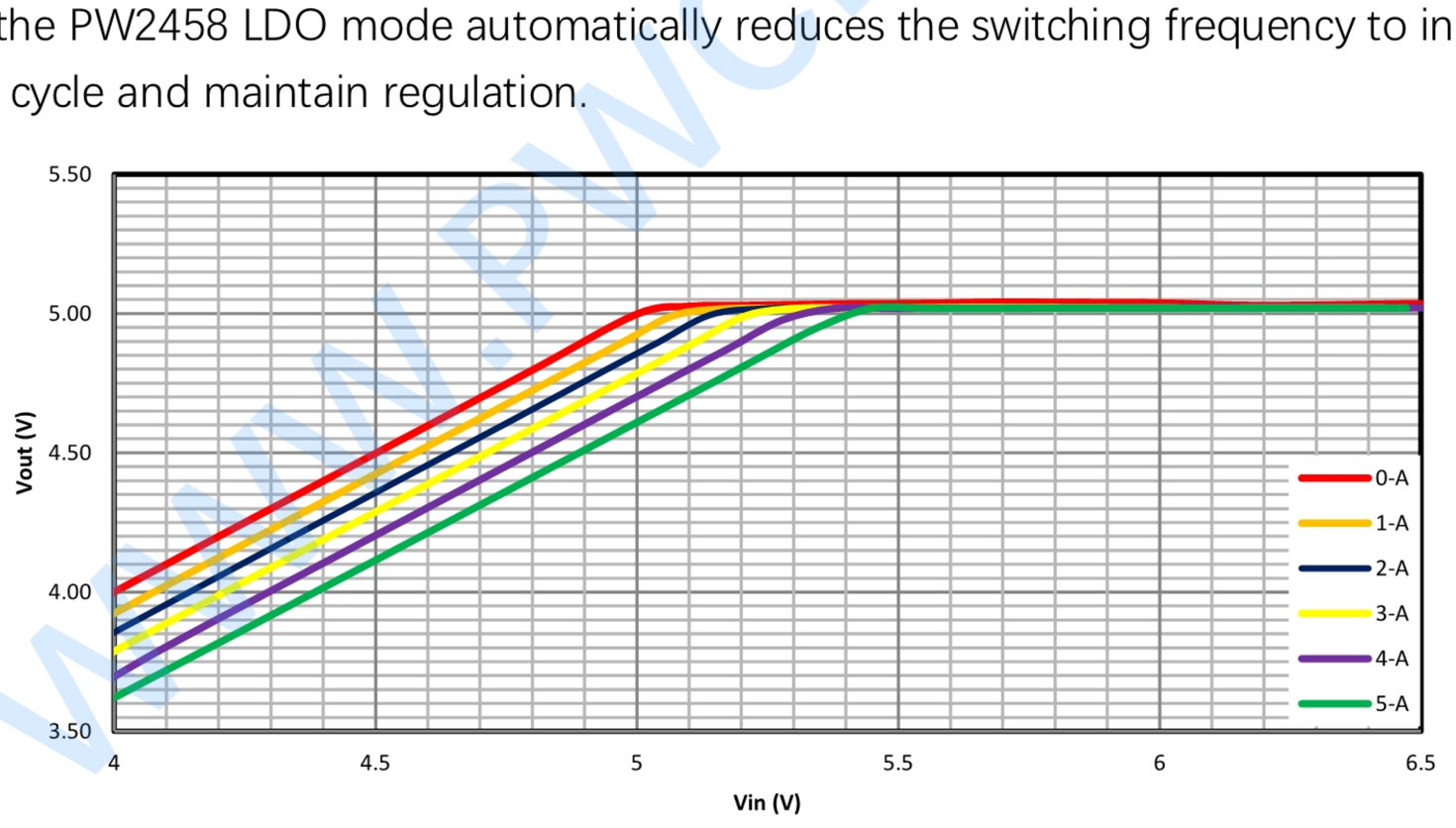
An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The UVLO of high-side MOSFET gate driver has rising threshold of 2.7V and hysteresis of 350mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be

not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.35V, BOOT UVLO occurs. The converter forces turning on low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range.

During the condition of ultra-low voltage difference from the input to the output, PW2458 operates in Low Drop-Out LDO mode. High-side MOSFET remains turning on as long as the BOOT pin to SW pin voltage is higher than BOOT UVLO threshold 2.7V. When the voltage from BOOT to SW drops below 2.4V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Low-side MOSFET only turns on for 100ns in each refresh cycle to minimize the output voltage ripple. Low-side MOSFET may turn on for several times till the bootstrap voltage is charged to higher than 2.7V for high-side MOSFET working normally. The effective duty cycle of the converter during LDO operation can be approaching to 100%

During slowing power up and power down application, the output voltage can closely track the input voltage ramping down thanks to LDO operation mode. As the input voltage is reduced to near the output voltage, i.e. during slowing power-up and power-down application, the off-time of the high side MOSFET starts to approach the minimum value. Without LDO operation mode, beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem the PW2458 LDO mode automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation.



LDO Operation Characteristic (Vout =5V)

Over Current Limit and Hiccup Mode

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The PW2458 implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The COMP pin voltage ramps up to high clamp voltage 3.7V typical. When COMP voltage is clamped for

512 cycles, the converter stops switching. After remaining OFF for 8192 cycles, the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high for 512 cycles, the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation. The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

Over voltage Protection

The PW2458 implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 110% of internal 0.8V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase. When the FB pin voltage falls below 105% of the 0.8V reference voltage, the high-side MOSFET can turn on again.

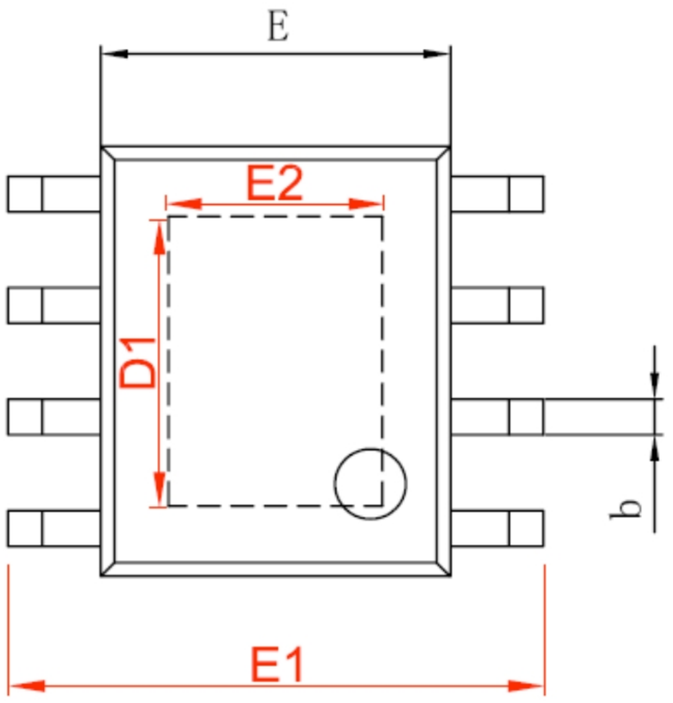
Thermal Shutdown

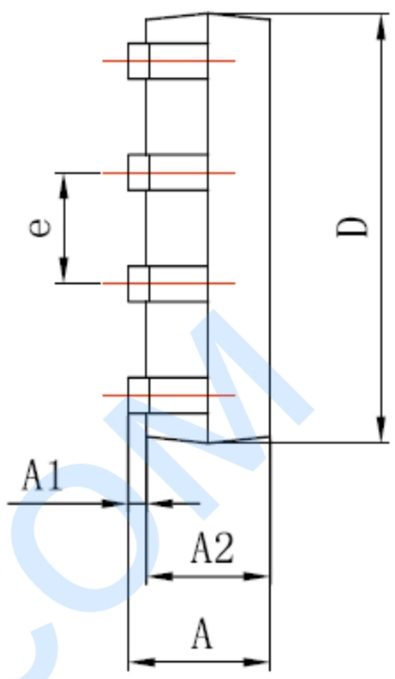
The PW2458 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 170C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 145C, the device restarts with internal soft start phase.

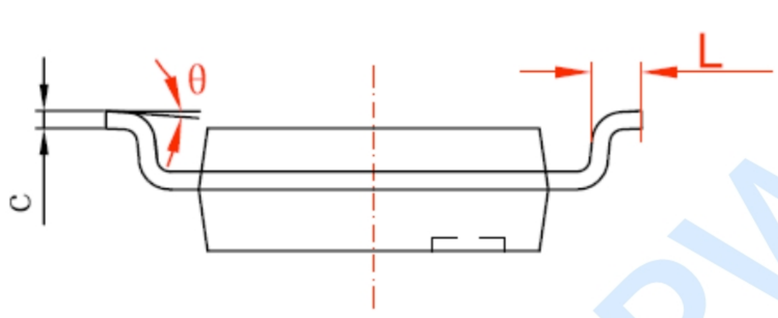
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PACKAGE INFORMATION

SOP8-EP







字符	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.002	0.006
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

Preliminary and all contents are subject to change without prior notice.

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