3A , 4.5V-30V Input , synchronous Step Down Regulator

General Description

PW2330 develops a high efficiency synchronous step down DC-DC converter capable of delivering 3A output current. PW2330 operates over a wide input voltage range from 4.5V to 30V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. PW2330 adopts the proprietary instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500kHz under continuous conduction mode to minimize the size of inductor and capacitor.

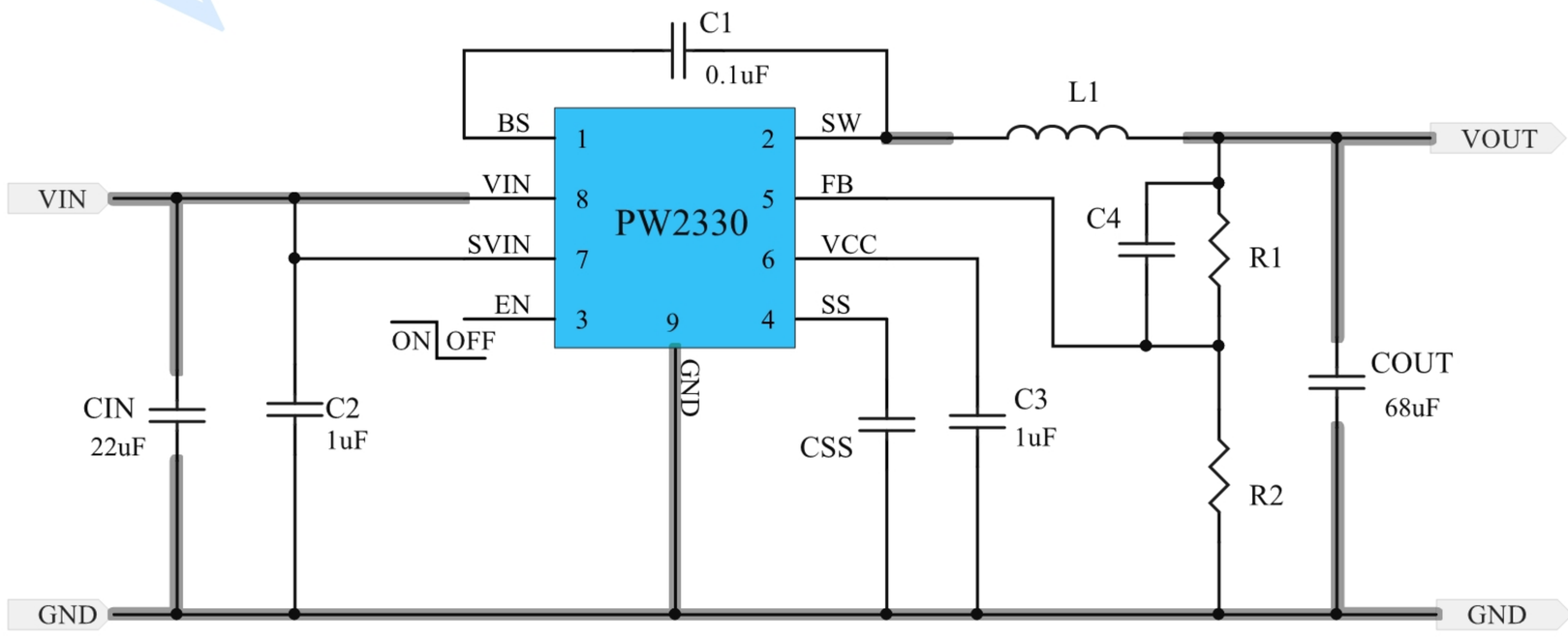
Features

- Low RDS(ON) for internal switches (top/bottom): 90/60 mΩ
- 4.5-30V input voltage range
- Instant PWM architecture to achieve fast transient responses
- External softstart limits the inrush current
- Pseudo-constant frequency: 500kHz
- 3A continuous load current capability
- Output over current limit
- Output short circuit protection with current fold back
- Thermal shutdown and auto recovery
- RoHS Compliant and Halogen Free
- Compact package: SOP8-EP

Applications

- LCD Monitor
- LCD-TV
- SetTop Box
- NAS
- High power AP router
- LCD Monitor
- DVR/NVR
- Notebook

TYPICAL APPLICATION CIRCUIT

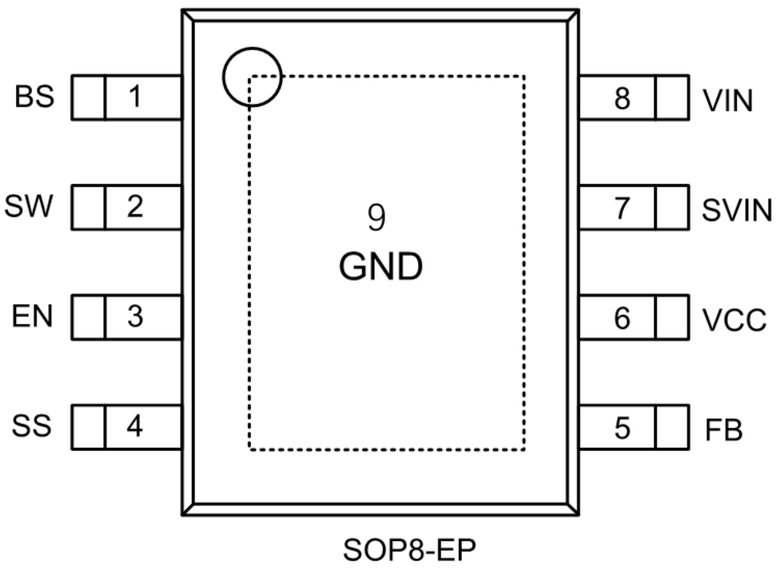


Tss(ms)=Css(nF)*0.6(V)/10(uA)

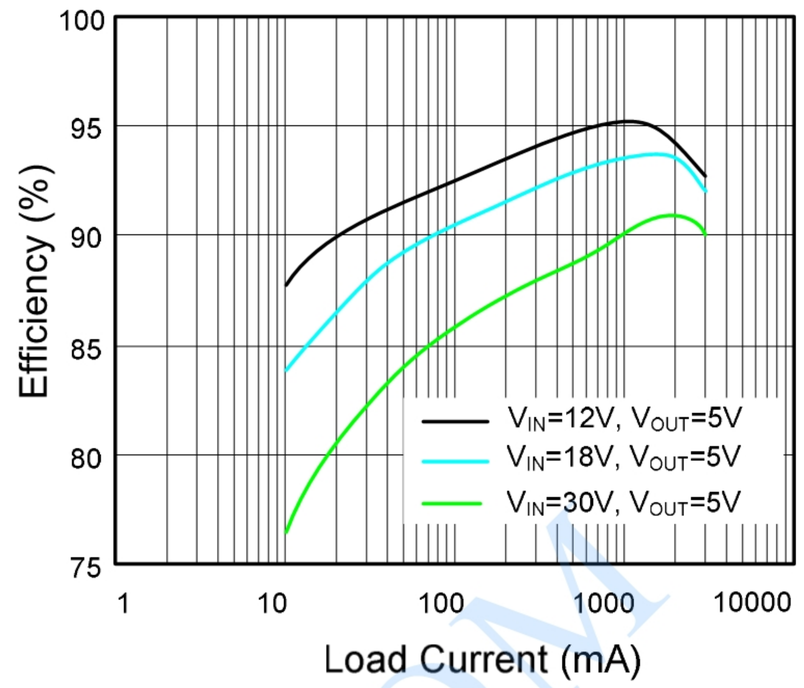
Vout=0.6*(1+R1/R2)，If：R1=100K,R2=22.1K，VOUT=3.3V

WWW.PWCHIP.COM

PIN ASSIGNMENT/DESCRIPTION



SOP8-EP



Pin Number	Pin Name	Function
1	BS	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to SW pin with 0.1uF ceramic cap.
2	SW	Inductor pin. Connect this pin to the switching node of inductor
3	EN	Enable control.
4	SS	Softstart programming pin. Connect a capacitor from this pin to ground to program the softstart time. **Tss(ms)=Css(nF)*0.6(V)/10(uA)**
5	FB	Output Feedback Pin. Connect this pin to the center point of the output resistor divider to program the output voltage: $\boldsymbol{Vout = 0.6 * (1 + R1/R2)}$
6	VCC	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Add a 1uF bypass capacitor between this pin and GND.
7	SVIN	Analog supply input. Bypass a 1uF capacitor to ground.
8	VIN	Power supply input. Decouple this pin to GND pin with at least 10uF ceramic cap
9(EP)	GND	Ground pin.

Recommended Operating Conditions (Note 3)

Parameter	VALUE
Supply Input Voltage	4.5V to 30V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C

WWW.PWCHIP.COM

Absolute Maximum Ratings (Note 1)

Parameter		VALUE	Unit
VIN, SVIN, SW, BS, EN		33	V
VCC, FB, SS, BS-SW		4	V
Power Dissipation, PD @ TA = 25°C		3.3	V
Package Thermal Resistance (Note 2)	θJA	30	°C/W
	θJC	10	°C/W
Junction Temperature Range		-40 to 150	°C
Lead Temperature (Soldering, 10 sec.)		260	°C
Storage Temperature Range		-65 to 85	°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θJA is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of SOP8-EP packages is the case position for θjc measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Layout Design:

The layout design of PW2330 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following componentsclose to the IC: CIN, C3 L1, R1 and R2.

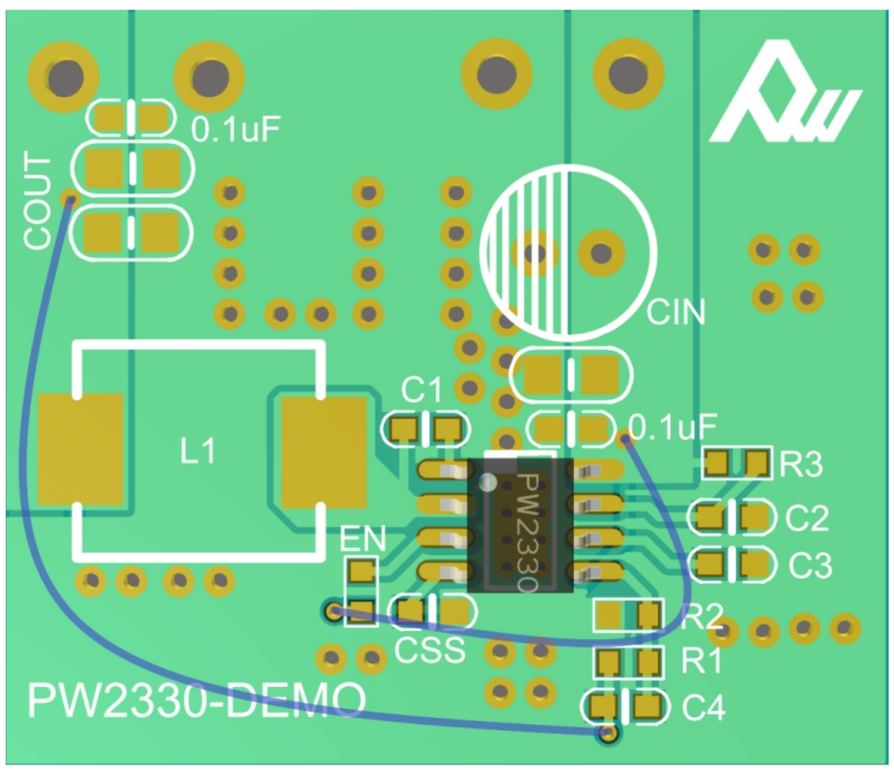
1, It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2, CIN must be close to VIN and GND Pins. The loop area formed by CIN and GND must be minimized.

3, The PCB copper area associated with SW pin must be minimized to avoid the potential noise problem.

4, The components R1 and R2, and the trace connecting to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise problem.

5, If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.



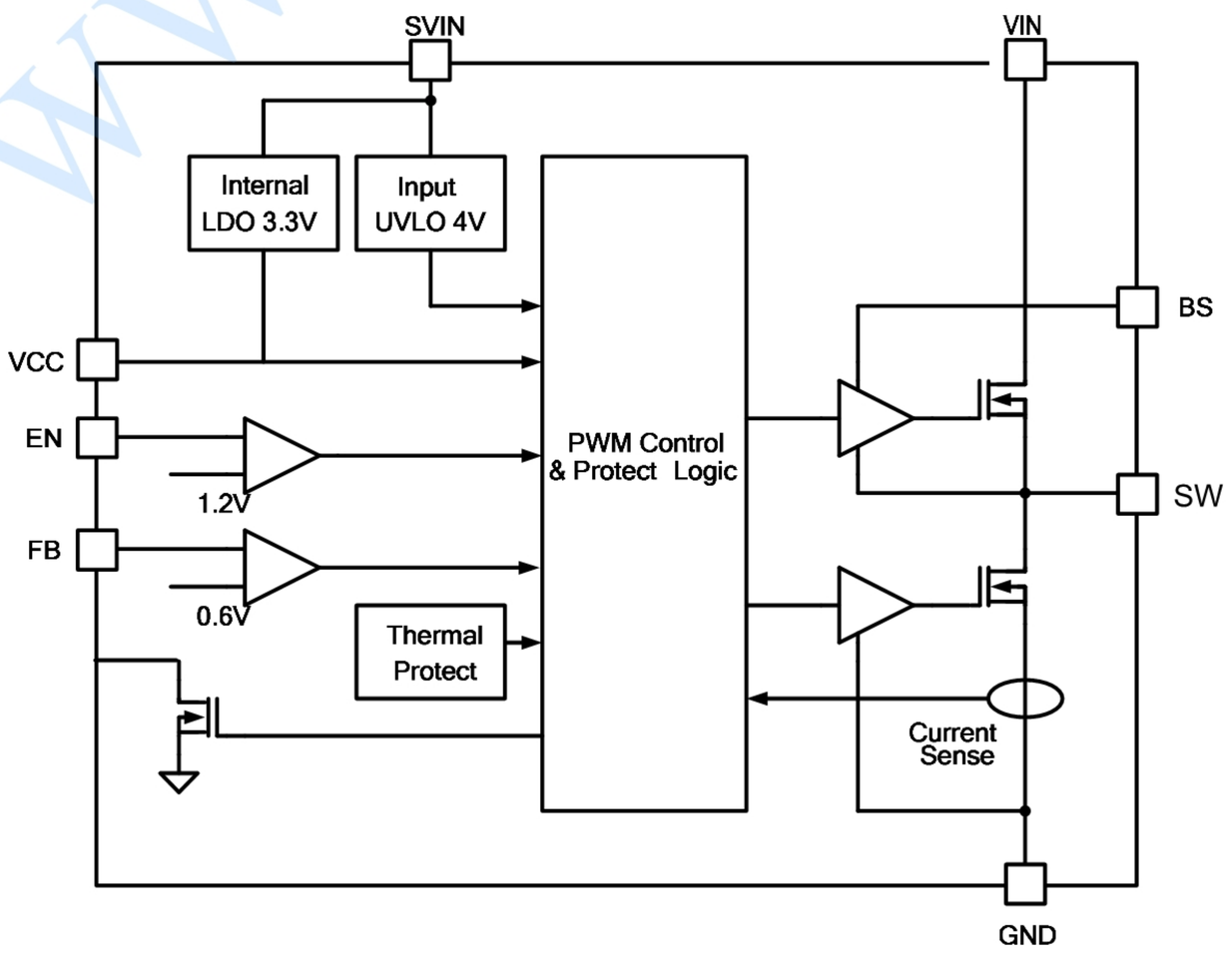
WWW.PWCHIP.COM

ELECTRICAL CHARACTERISTICS

(VIN = 12V, VOUT = 5V, COUT = 47uF, TA = 25°C, IOUT = 1A unless otherwise specified.)

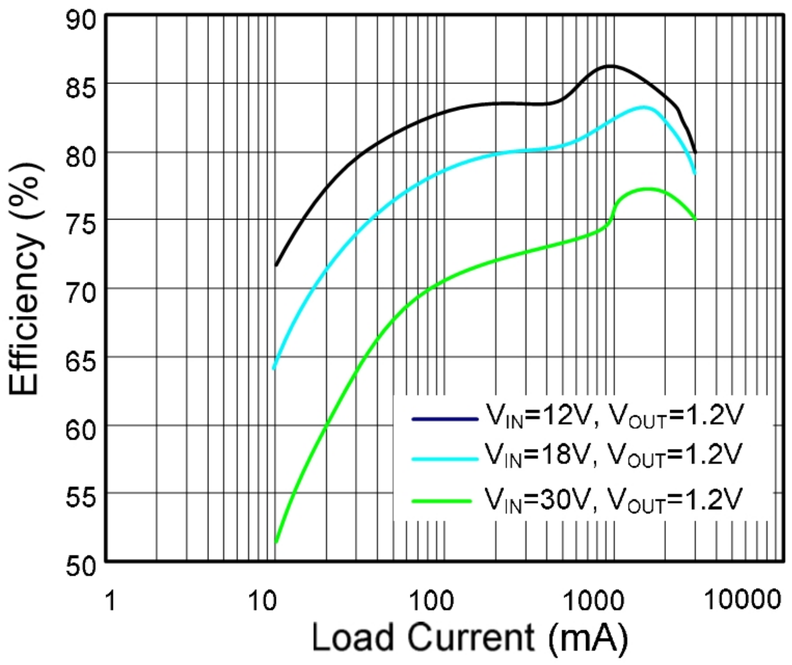
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	VIN		4.5		30	V
Quiescent Current	IQ	IOUT=0,VFB=VREF*105%		200		μA
Shutdown Current	ISHDN	EN=0		5	10	μA
Feedback Reference Voltage	VREF		0.591	0.6	0.609	V
FB Input Current	IFB	VFB=Vcc	-50		50	nA
Top FET RON	RDS(ON)1			90		mΩ
Bottom FET RON	RDS(ON)2			60		mΩ
Bottom FET Current Limit	ILIM		4			A
EN falling threshold	VENL		1.1	1.2	1.3	V
EN threshold hysteresis	VEN.HYS			0.1		V
Input UVLO threshold	VUVLO				4	v
UVLO hysteresis	VHYS			0.2		V
Oscillator Frequency	Fosc	IOUT=200mA		0.5		MHz
Min ON Time				80		ns
Min OFF Time				120		ns
Internal LDO Output	Vvcc	VIN=4V	3.2	3.2	3.4	V
Thermal Shutdown Temperature	TSD			160		°C
Thermal Shutdown Hysteresis	TSD,HYS			20		°C

Function Block

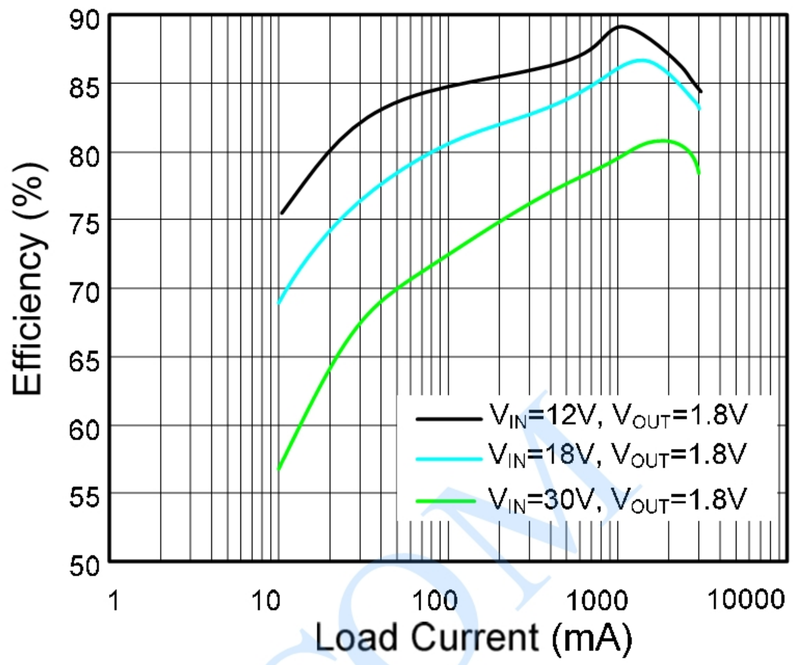


WWW.PWCHIP.COM

Typical Performance Characteristics

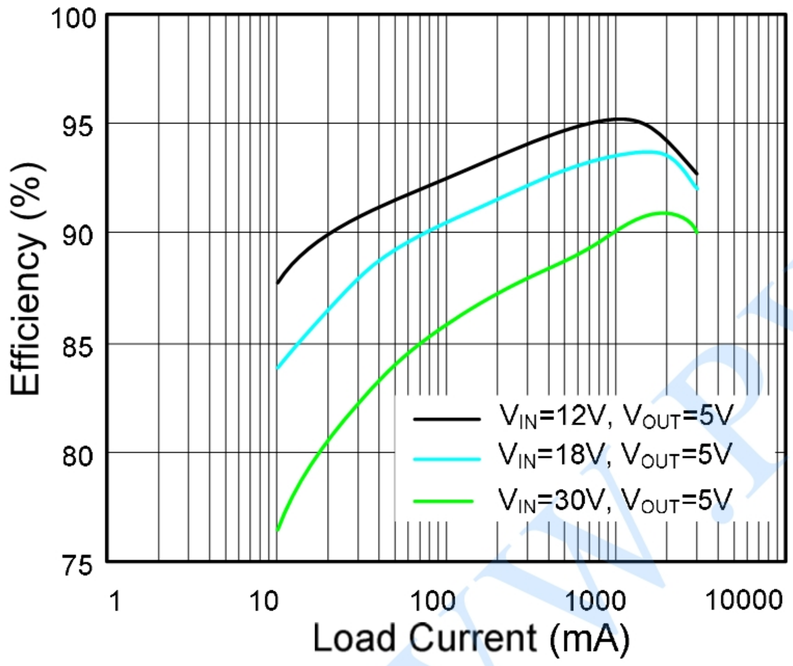


Efficiency vs. Load Current

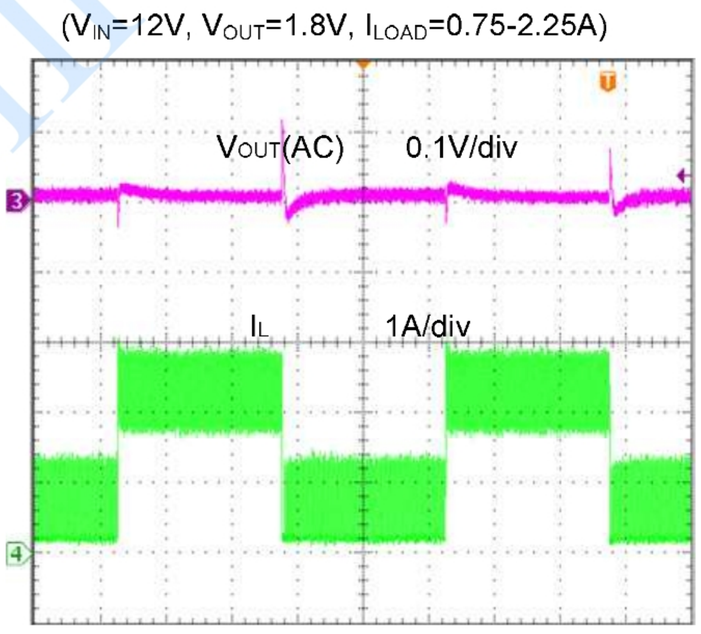


Efficiency vs. Load Current

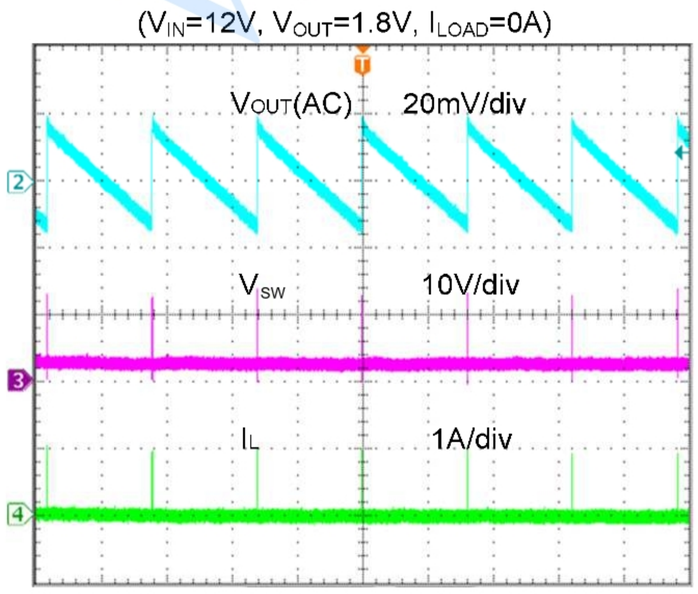
.



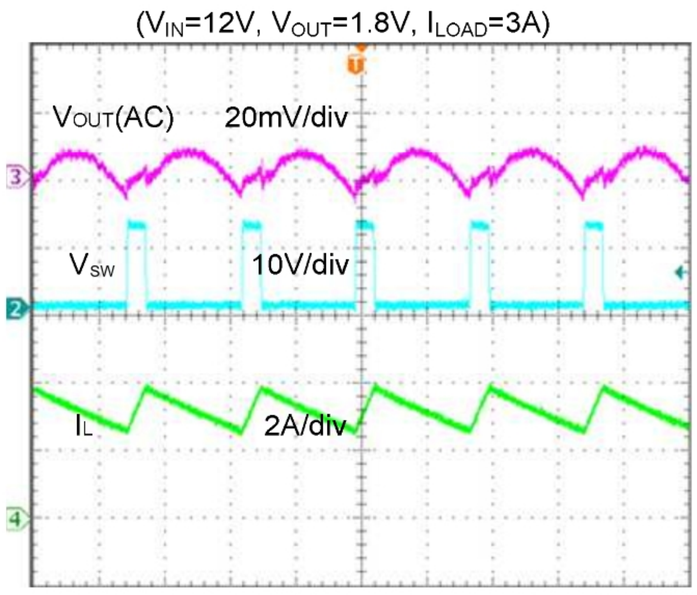
Efficiency vs. Load Current



Load Transient



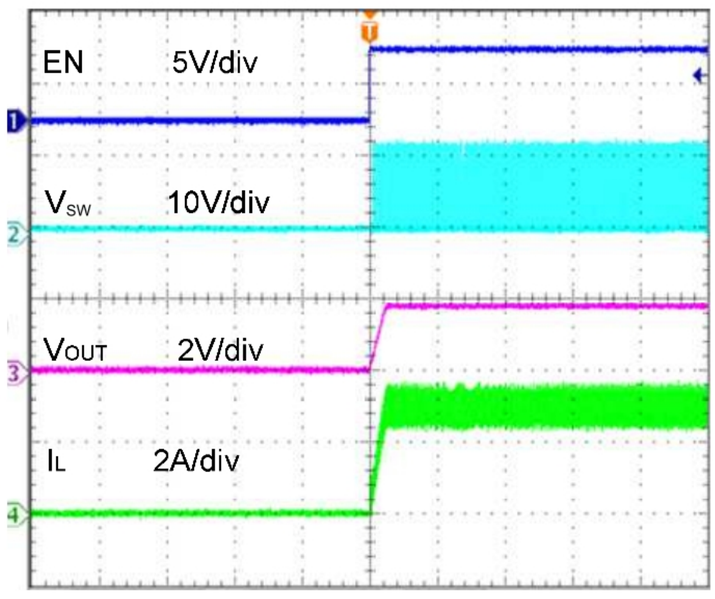
Output Ripple



Output Ripple

WWW.PWCHIP.COM

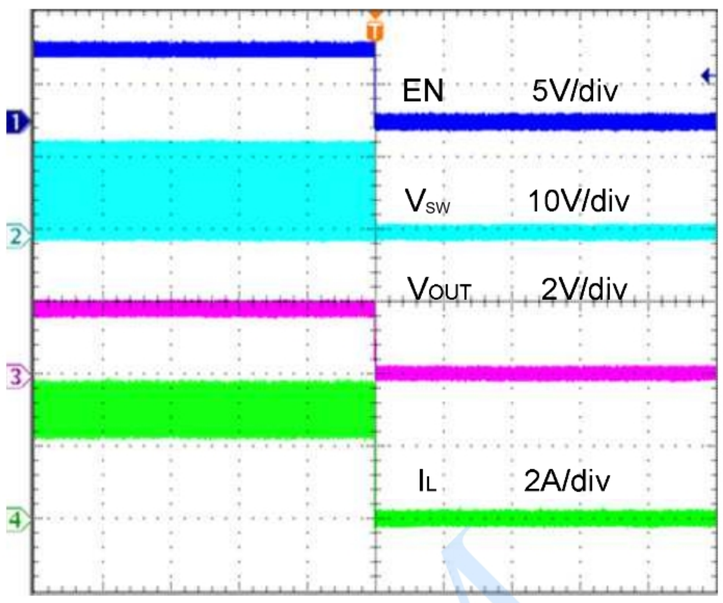
(V_{IN}=12V, V_{OUT}=1.8V, I_{LOAD}=3A)



Time (10ms/div)

Startup

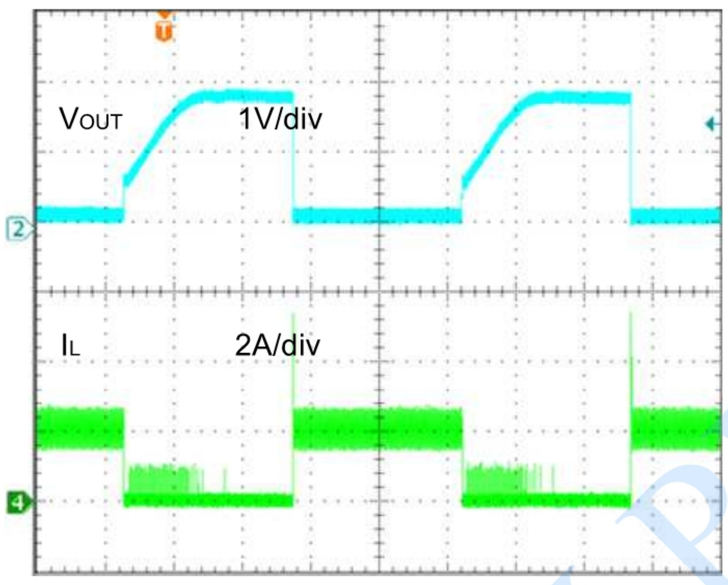
(V_{IN}=12V, V_{OUT}=1.8V, I_{LOAD}=3A)



Time (10ms/div)

Shutdown

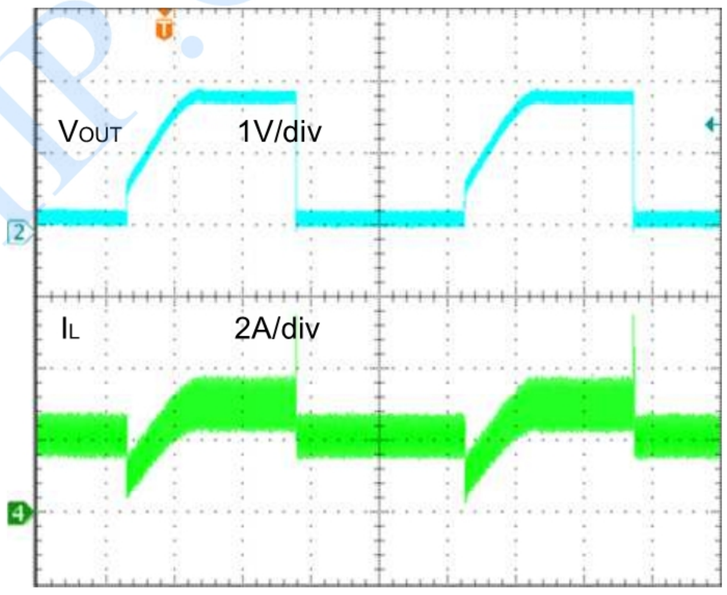
(V_{IN}=12V, V_{OUT}=1.8V, 0A to Short)



Time (2ms/div)

Short Circuit Protection

(V_{IN}=12V, V_{OUT}=1.8V, 3A to Short)



Time (2ms/div)

Short Circuit Protection

Operation

PW2330 is a synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low Rds(on) power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint. PW2330 provides protection functions such as cycle by cycle current limiting and thermal shutdown protection. PW2330 will sense the output voltage conditions for the fault protection.

WWW.PWCHIP.COM

Applications Information

Because of the high integration in the PW2330 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor CIN, output capacitor COUT, output inductor L and feedback resistors (R1 and R2) need to be selected for the targeted applications specifications.

Feedback Resistor Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If Vout is 3.3V, R1=100k is chosen, then using following equation, R2 can be calculated to be 22.1k:

$$VOUT = \left(1 + \frac{R1}{R2}\right) * 0.6$$

Enable Operation

Pulling the EN pin low (<1.2V) will shut down the device. During shutdown mode, the PW2330 shutdown current drops to lower than 5uA, Driving the EN pin high (>1.3V) will turn on the IC again.

External Bootstrap Capacitor

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between BS pin and SW pin is recommended.

VCC LDO

The 3.3V LDO is for internal analog circuit and driving circuit. Bypass this pin to ground with a 1uF ceramic capacitor. The VCC LDO is capable of sourcing 20mA current.

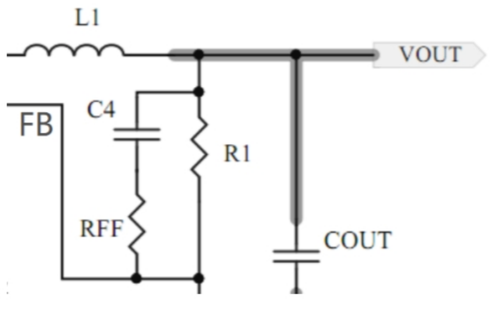
Soft-start

Connect a capacitor from softstart programming pin to ground to program the softstart time.

Tss(ms)=Css(nF)*0.6(V)/10(uA)

Load Transient Considerations

The PW2330 regulator IC adopts the instant PWM architecture to achieve good stability and fast transient responses. In applications with high step load current, adding an RC network RFF and C4 parallel with R1 may further speed up the load transient responses.



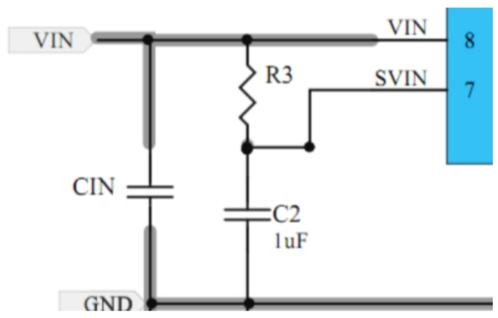
WWW.PWCHIP.COM

Input capacitor CIN:

The ripple current through input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \sqrt{D(1-D)} \cdot$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the VIN and GND pins. Care should be taken to minimize the loop area formed by CIN, and VIN/GND pins. In this case, a 10uF low ESR ceramic capacitor is recommended.



The internal analog circuit is powered from SVIN. To avoid the noise issue, a 1uF ceramic capacitor connected closely from SVIN to GND is recommended. An RC filter can also be added from power input to SVIN.

Output capacitor COUT:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 47uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and IOUT,MAX is the maximum load current.

The PW2330 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

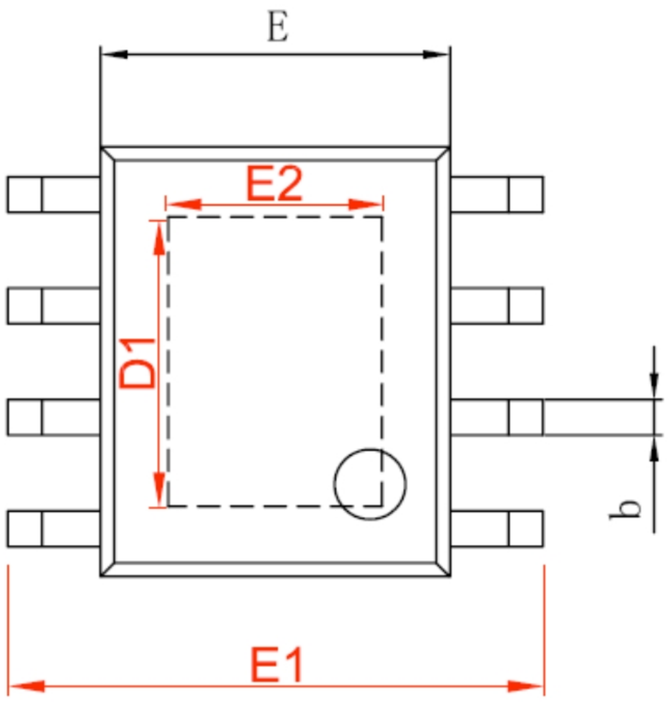
2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

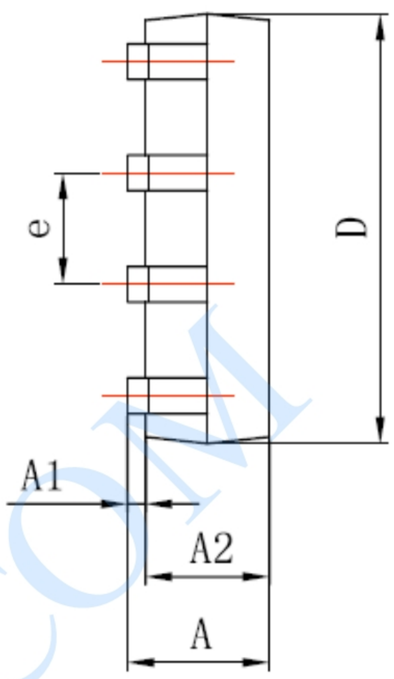
$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2\ F_{SW}\ L}$$

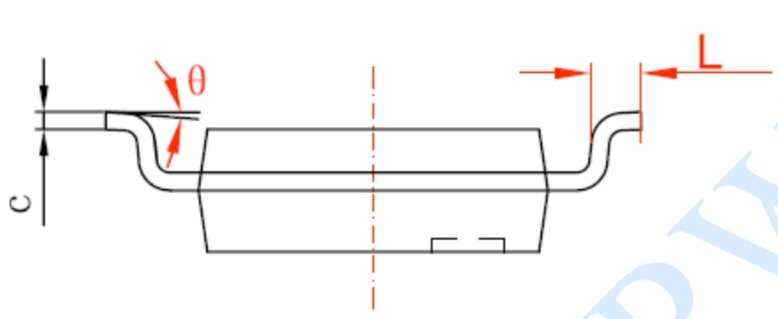
3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

PACKAGE DESCRIPTION

SOP8-EP







字符	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.002	0.006
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

Preliminary and all contents are subject to change without prior notice.

WWW.PWCHIP.COM

IMPORTANT NOTICE

Wuxi PWChip Semi Technology CO., LTD (PW) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any products or services. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

PW assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using PW components.

PW products are not authorized for use in safety-critical applications (such as life support devices or systems) where a failure of the PW product would reasonably be expected to affect the safety or effectiveness of that devices or systems.

The information included herein is believed to be accurate and reliable. However, PW assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

WWW.PWCHIP.COM