



## N-Channel Enhancement Mode MOSFET

### GENERAL DESCRIPTION

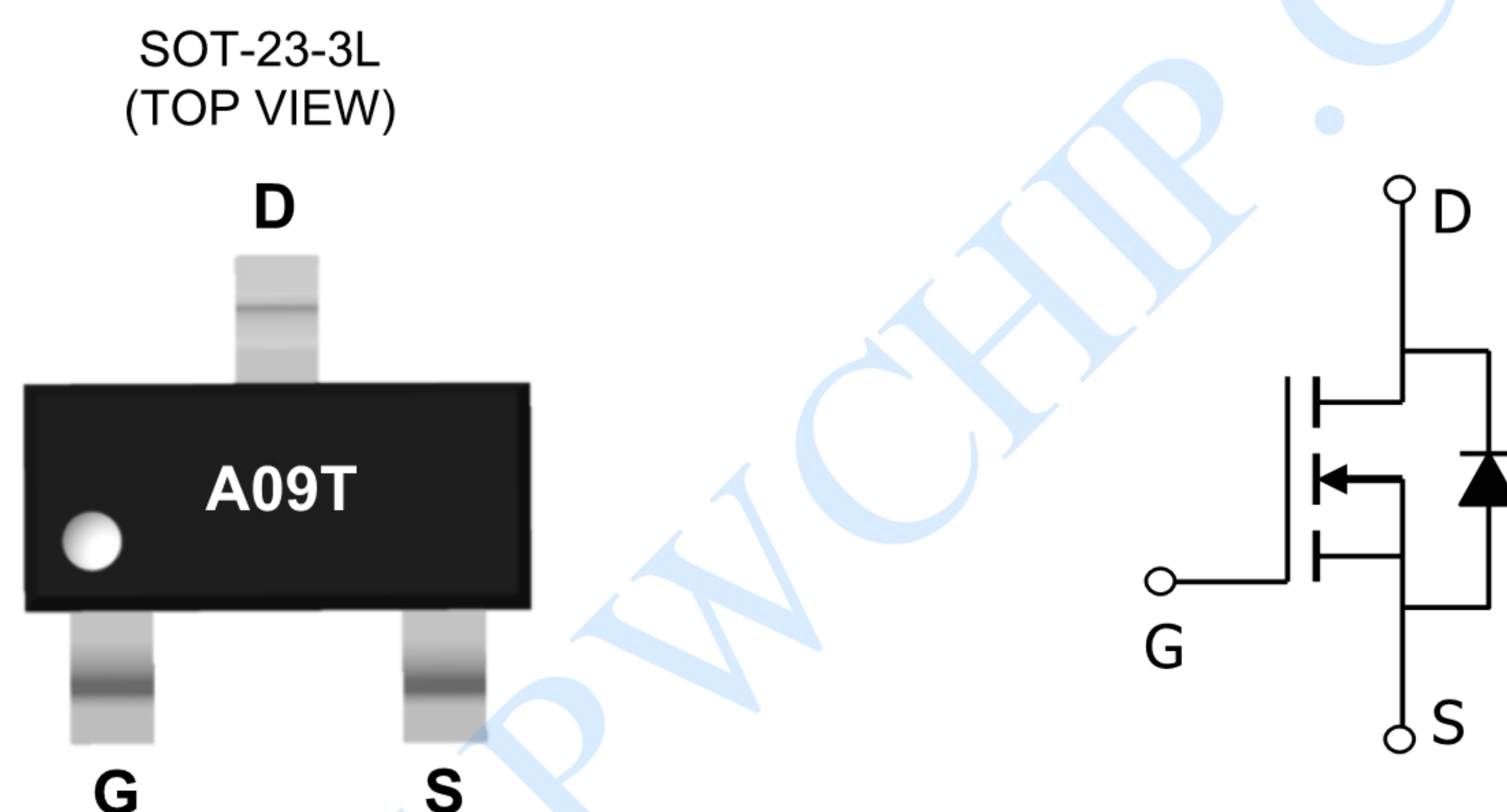
The PW3400A uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application..

### FEATURES

$V_{DS} = 30V$   $I_D = 5.8A$

$R_{DS(ON)} < 28m\Omega$  @  $V_{GS}=10V$

Available in a 3-Pin SOT23-3 Package



### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current	$I_{D@TA=25^{\circ}C}$	5.8	A
Continuous Drain Current	$I_{D@TA=70^{\circ}C}$	4.9	A
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	20	A
Total Power Dissipation <sup>3</sup>	$P_D@TA=25^{\circ}C$	1	W
Storage Temperature Range	$T_{STG}$	-55 To 150	°C
Operating Junction Temperature Range	$T_J$	-55 To 150	°C
Thermal Resistance Junction-ambient <sup>1</sup>	$R_{\theta JA}$	125	°C/W
Thermal Resistance Junction-Ambient 1 ( $t \leq 10s$ )	$R_{\theta JC}$	80	





## ELECTRICAL CHARACTERISTICS

(TA = 25°C, unless otherwise noted.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	30	33	---	V
ΔBVDSS/ΔT <sub>J</sub>	BVDSS Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =1mA	---	0.029	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =5.8A	---	20	28	mΩ
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V , I <sub>D</sub> =5A	---	24	32	mΩ
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =2.5V , I <sub>D</sub> =4A	---	31	55	mΩ
VGS(th)	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	0.5	0.85	1.2	V
ΔVGS(th)	V <sub>GS(th)</sub> Temperature Coefficient		---	-2.82	---	mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =24V , V <sub>GS</sub> =0V , T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =24V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±12V , V <sub>DS</sub> =0V	---	---	±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =5A	---	25	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz	---	1.5	---	Ω
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =15V , V <sub>GS</sub> =4.5V , I <sub>D</sub> =5.8A	---	11.5	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	1.6	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	2.9	---	
Td(on)	Turn-On Delay Time	V <sub>DD</sub> =15V , V <sub>GS</sub> =10V , R <sub>G</sub> =3Ω I <sub>D</sub> =5A	---	5	---	ns
T <sub>r</sub>	Rise Time		---	47.	---	
Td(off)	Turn-Off Delay Time		---	26	---	
T <sub>f</sub>	Fall Time		---	8	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz	---	860	---	pF
C <sub>oss</sub>	Output Capacitance		---	84	---	
Crss	Reverse Transfer Capacitance		---	70	---	
I <sub>s</sub>	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	---	---	5.8	A
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>s</sub> =1A , T <sub>J</sub> =25°C	---	---	1.2	V

### Note :

- 1、 The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

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## Typical Characteristics

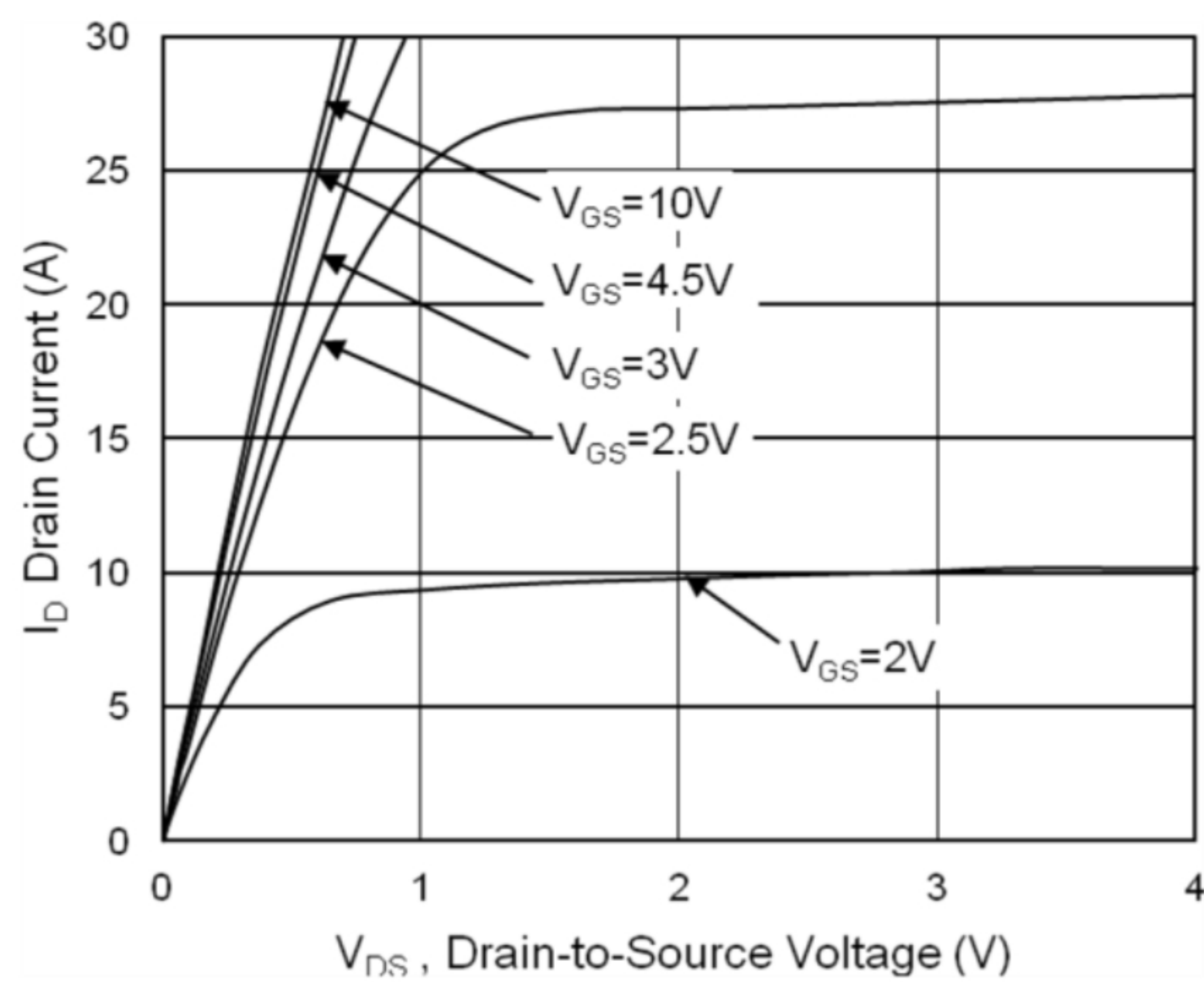


Fig.1 Typical Output Characteristics

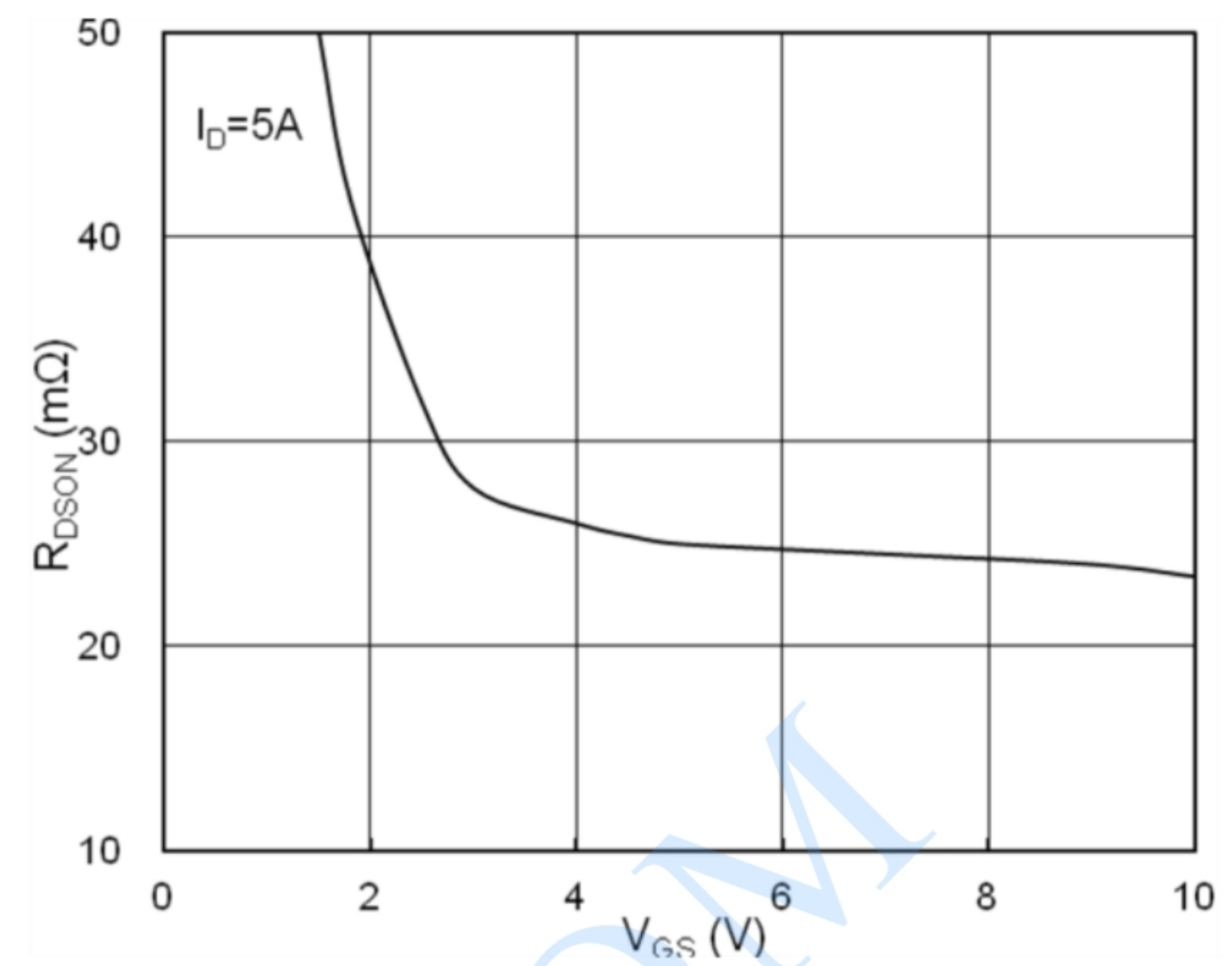


Fig.2 On-Resistance vs. Gate-Source

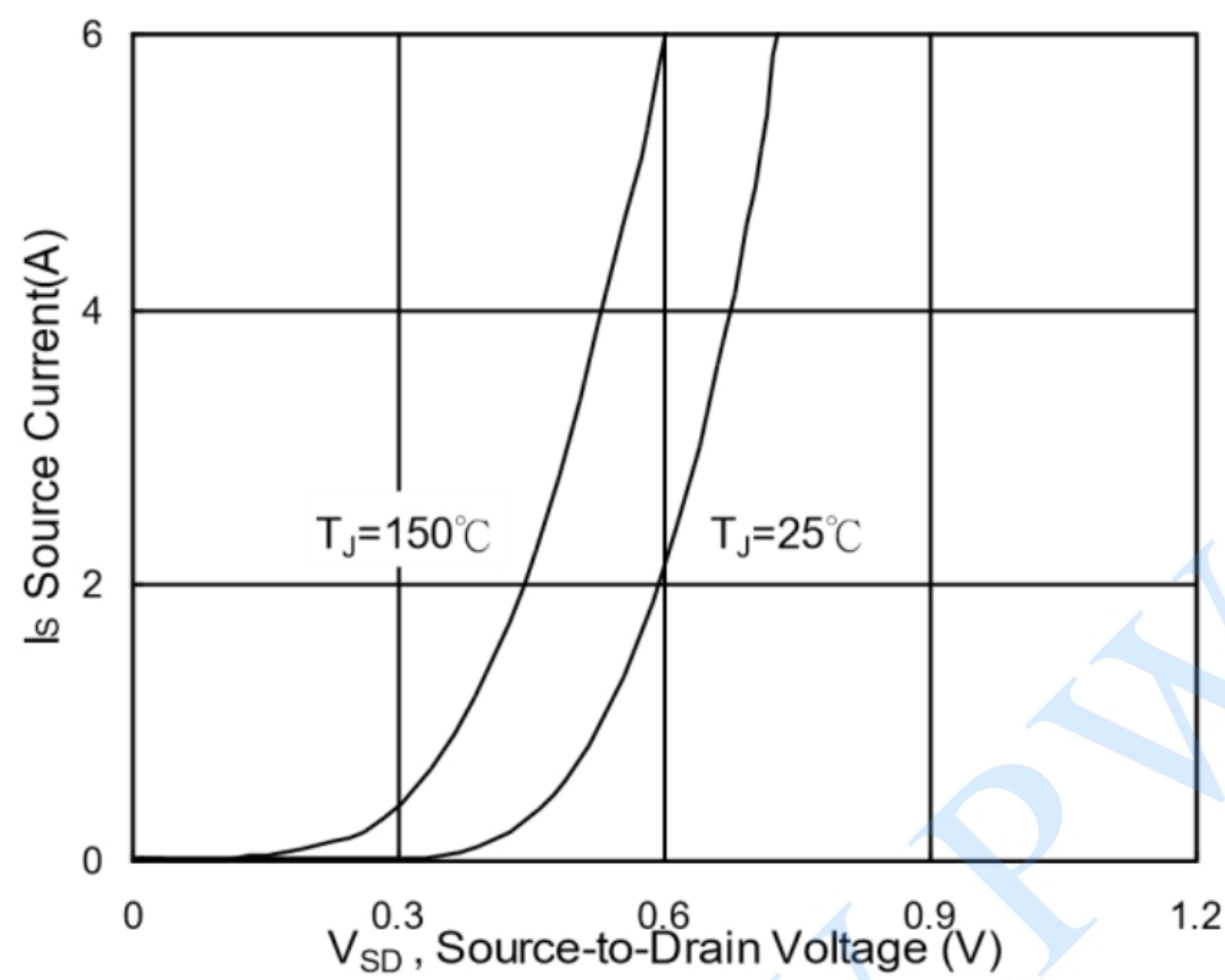


Fig.3 Forward Characteristics Of Reverse

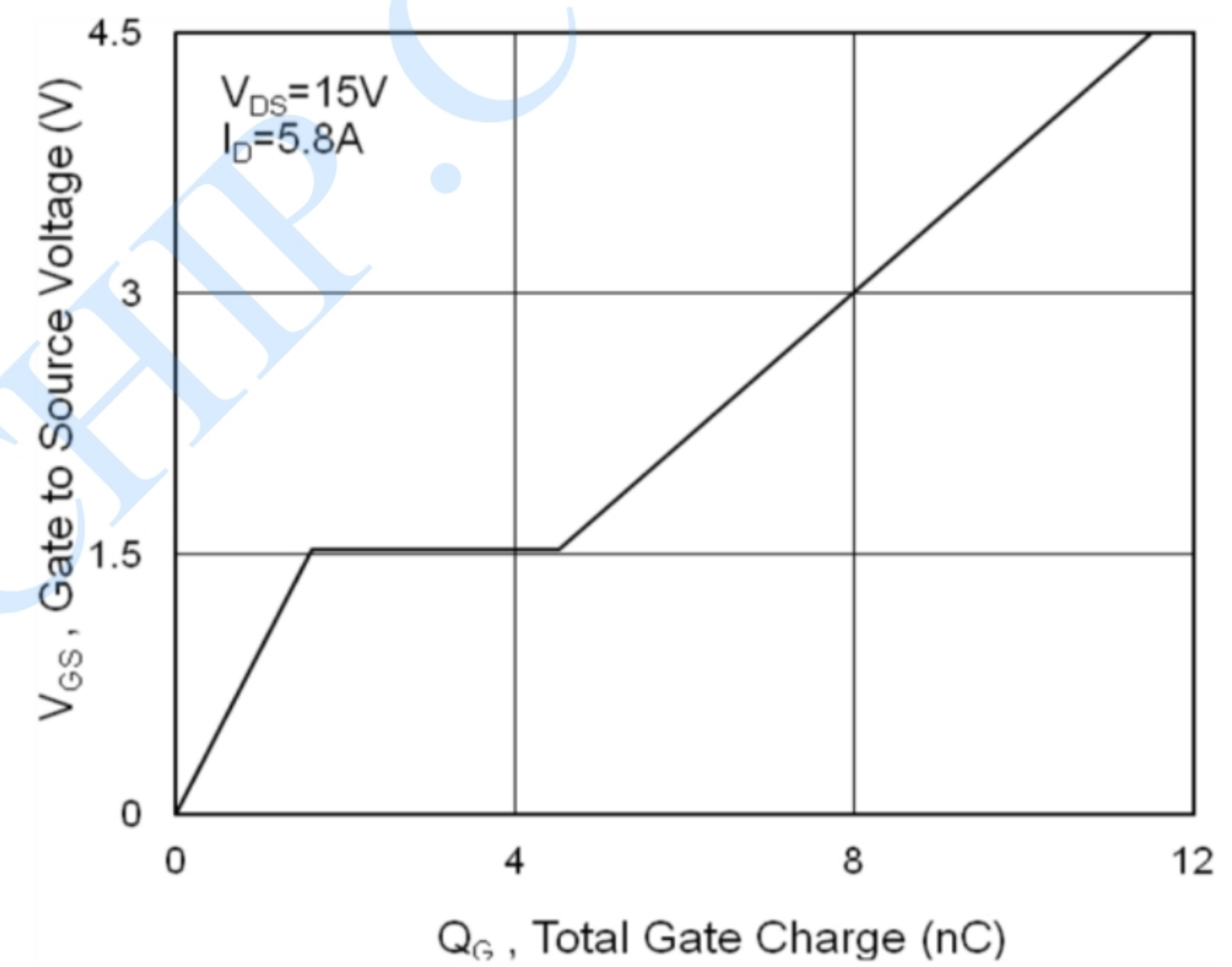


Fig.4 Gate-Charge Characteristics

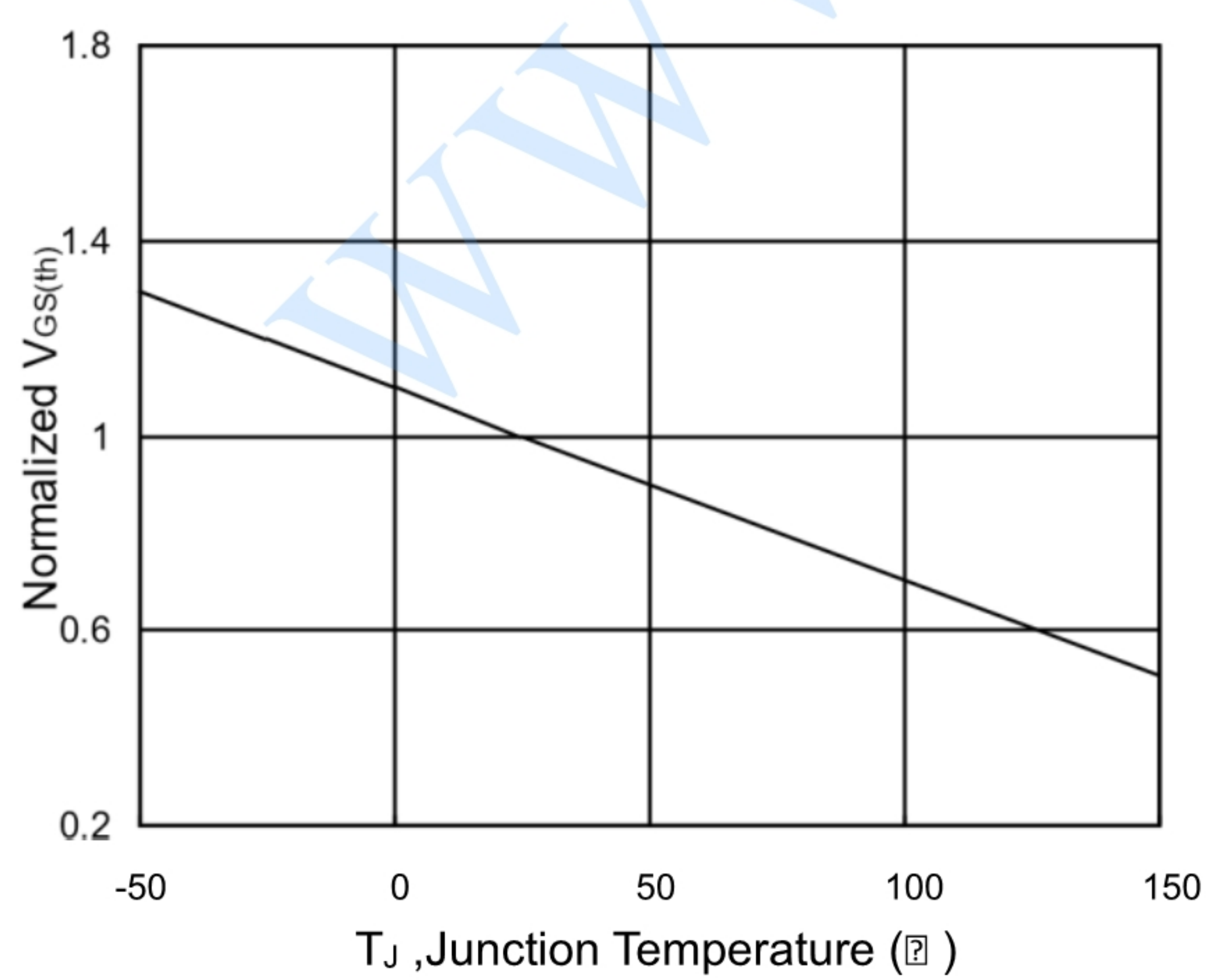


Fig.5 Normalized V\_GS(th) vs. T\_J

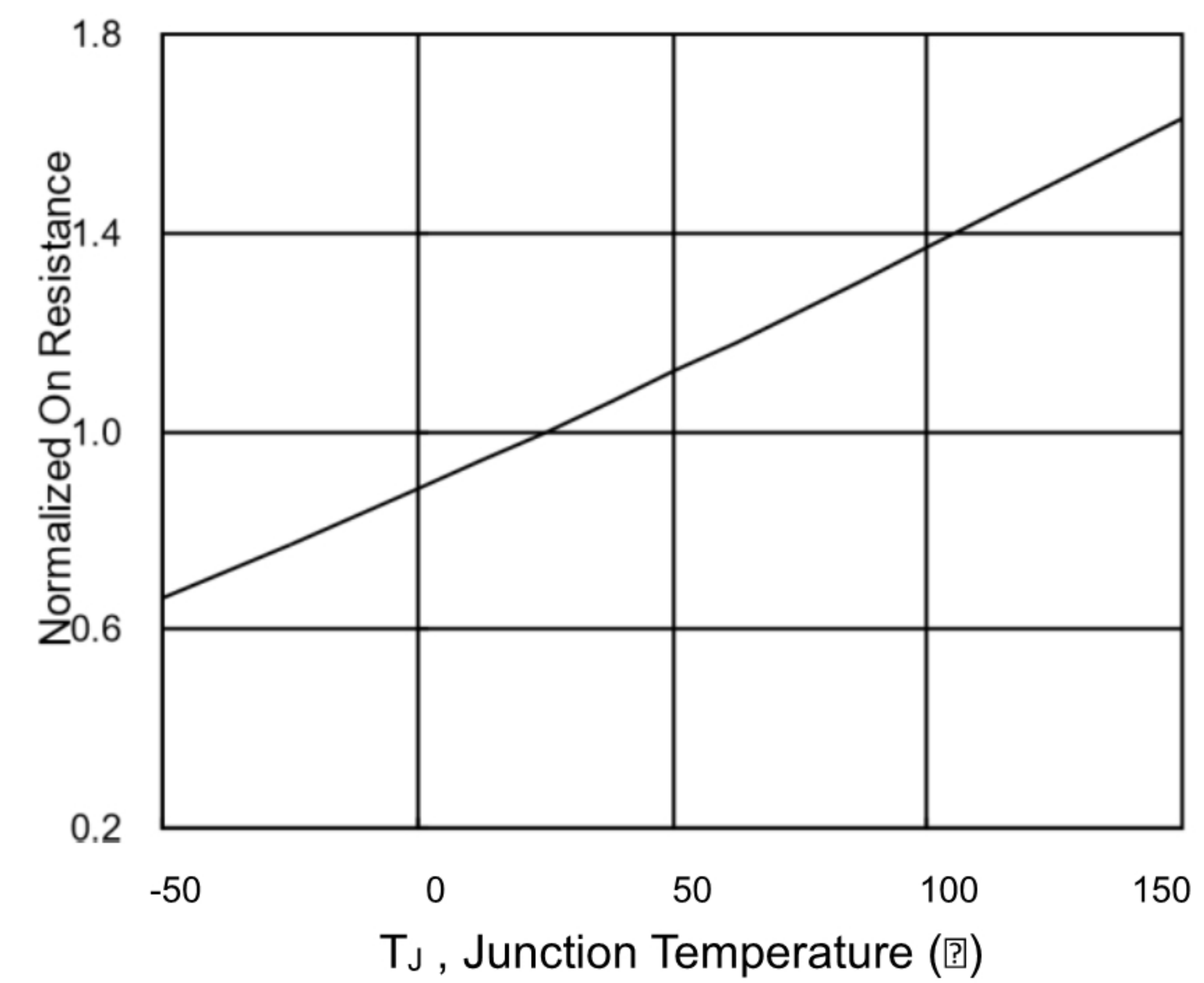


Fig.6 Normalized R\_DS(on) vs. T\_J



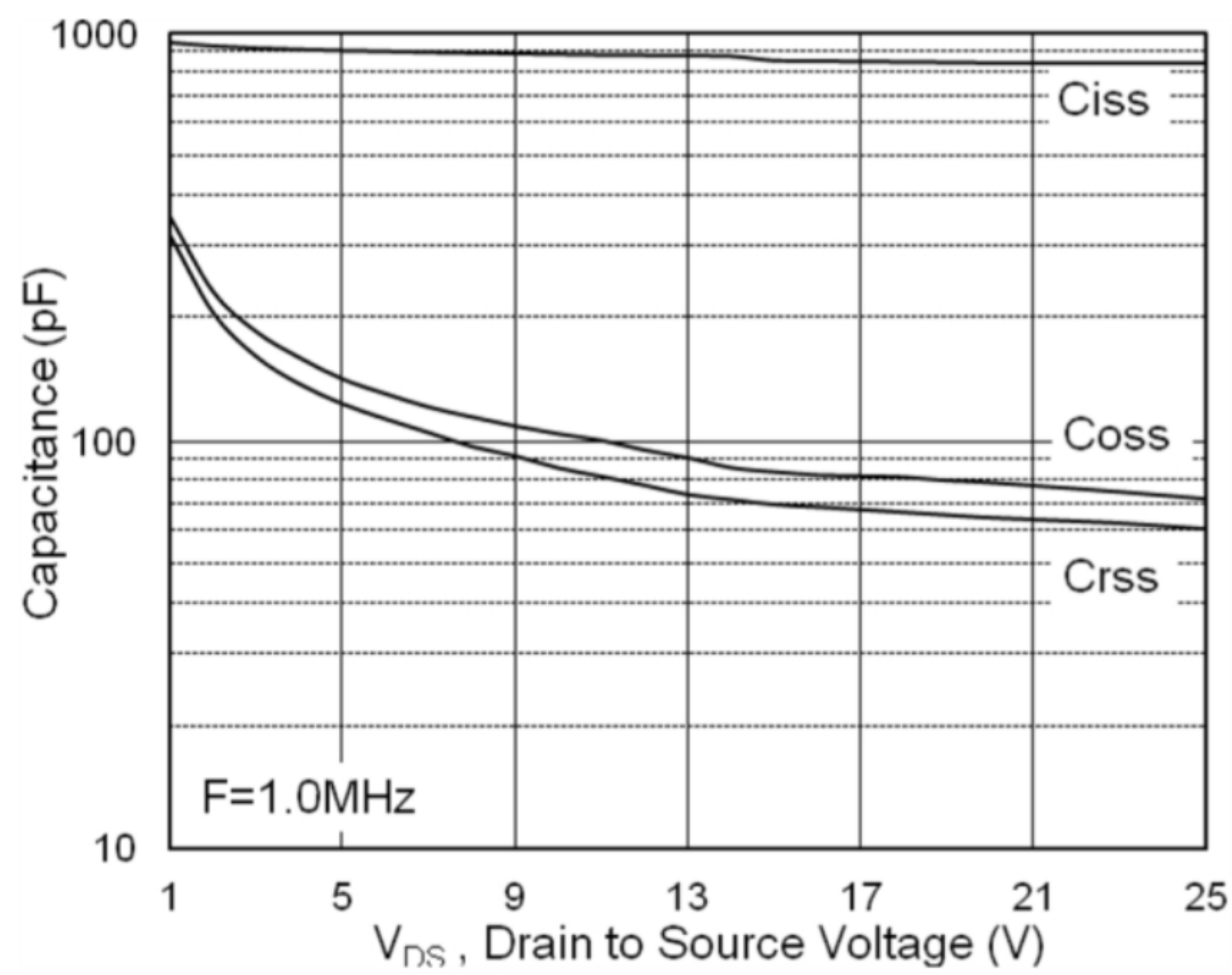


Fig.7 Capacitance

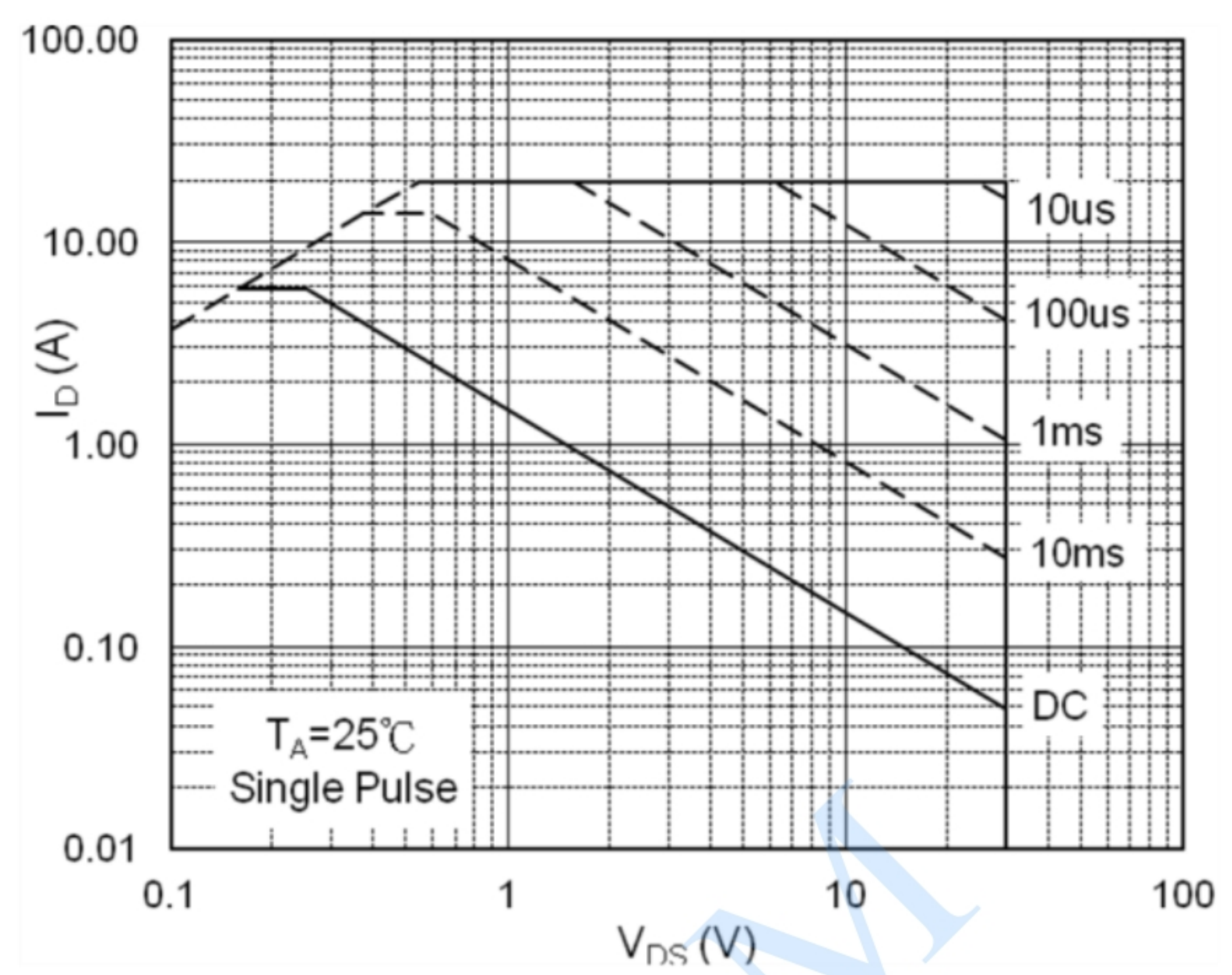


Fig.8 Safe Operating Area

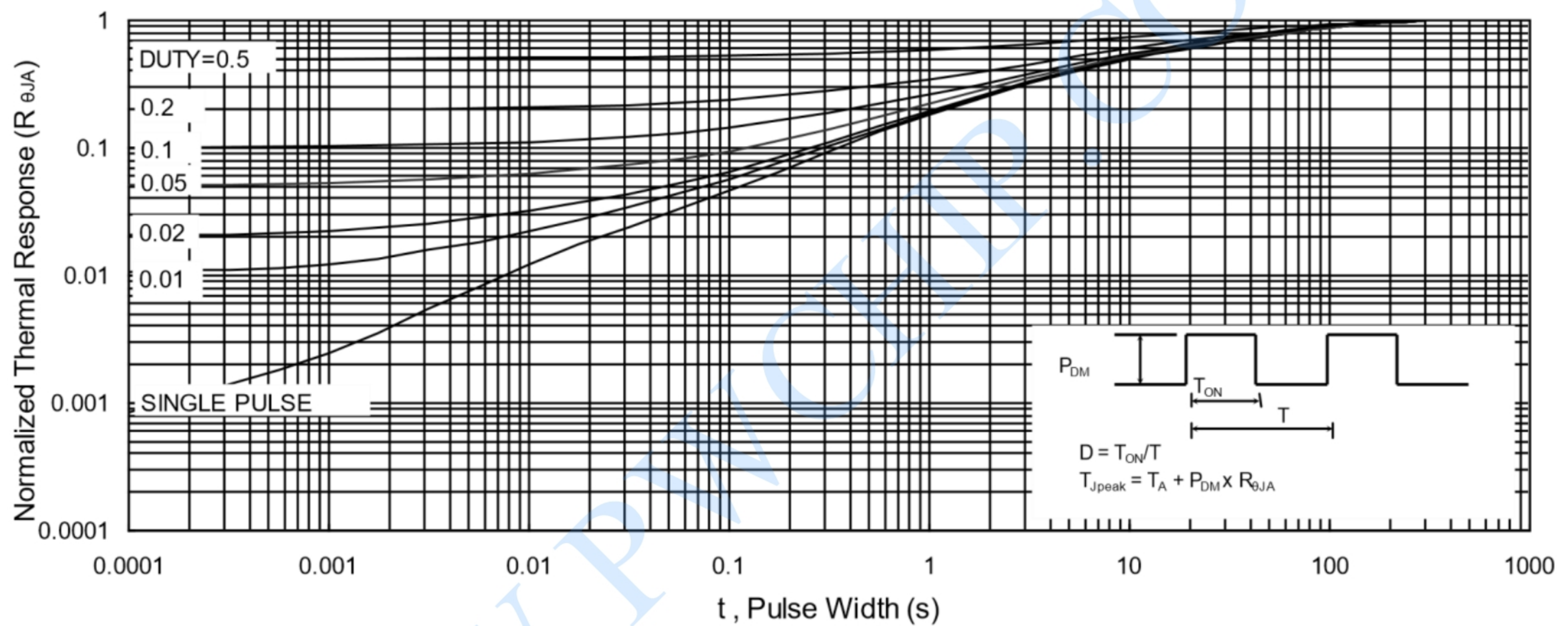


Fig.9 Normalized Maximum Transient Thermal Impedance

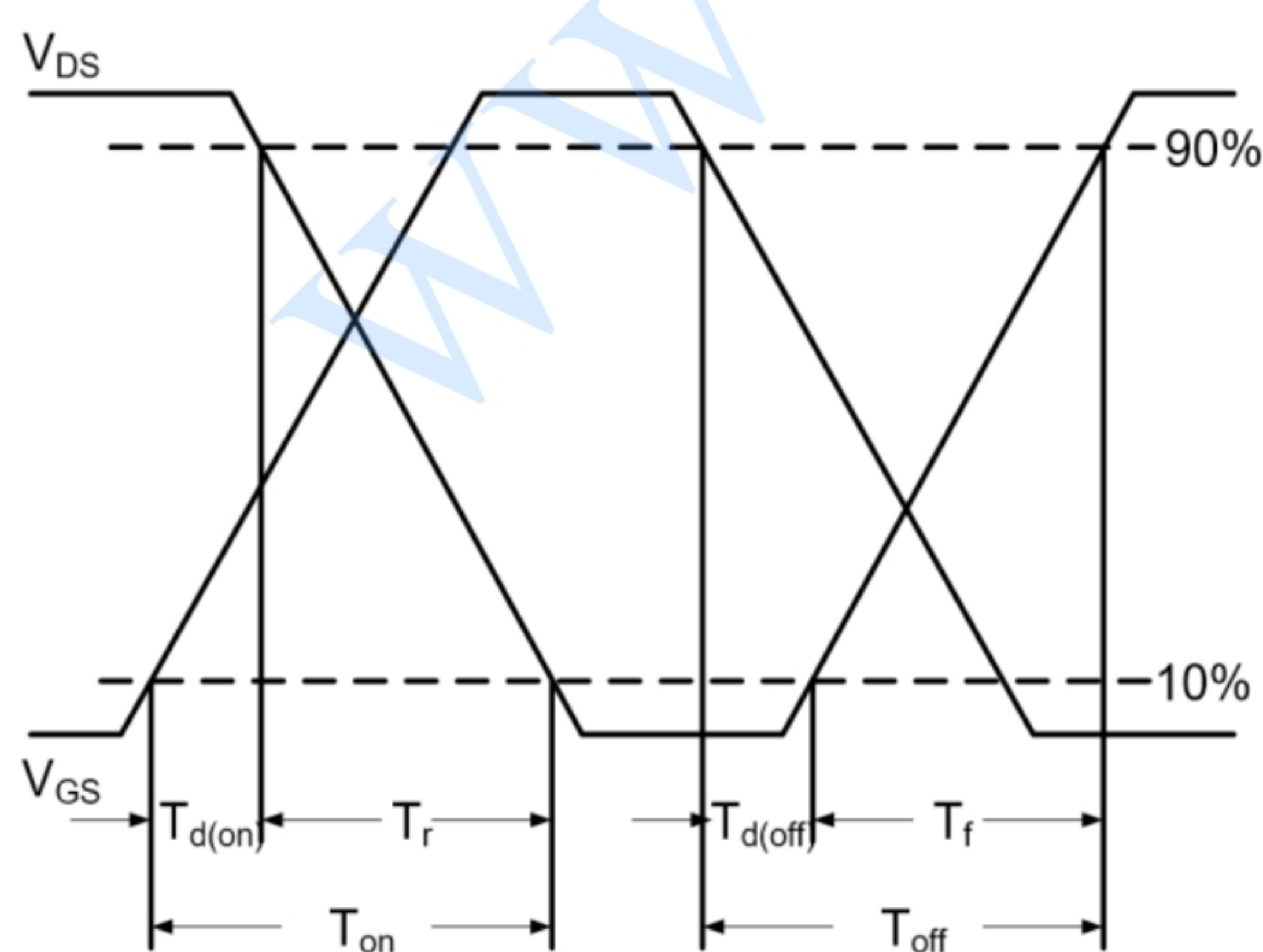


Fig.10 Switching Time Waveform

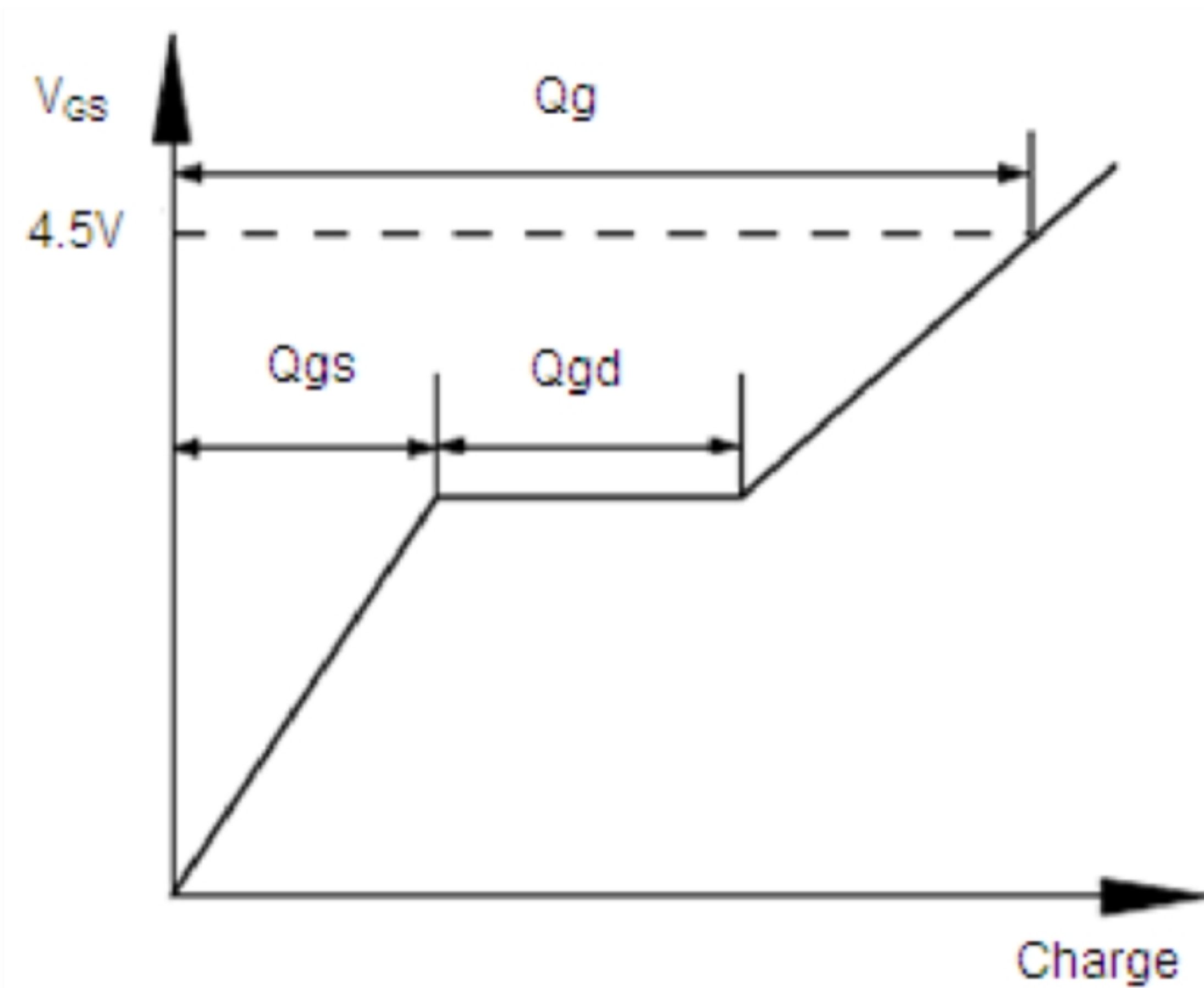
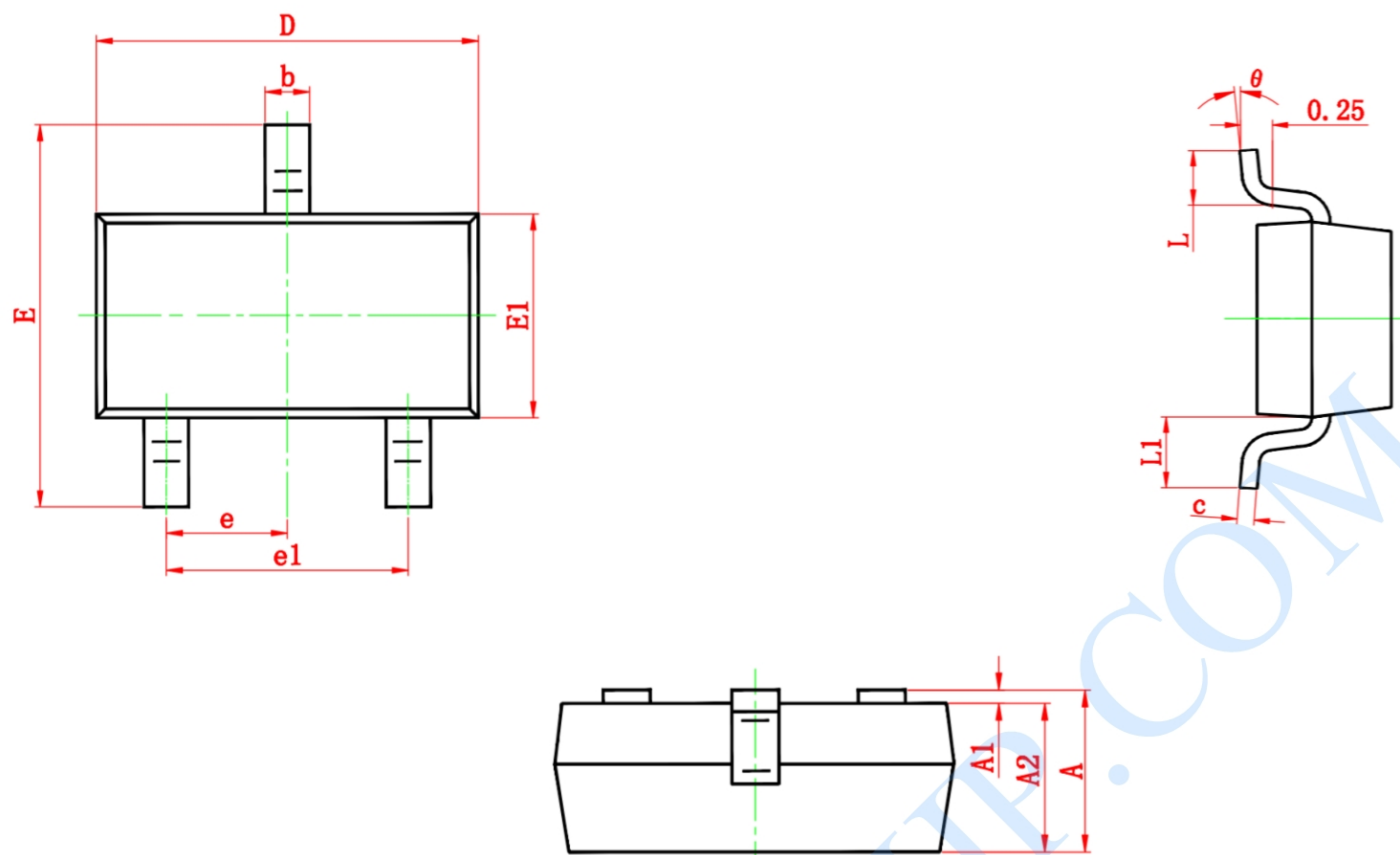


Fig.11 Gate Charge Waveform



## PACKAGE DESCRIPTION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	2.250	2.550	0.089	0.100
E1	1.200	1.400	0.047	0.055
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.300	0.500	0.012	0.020
L1	0.550 REF.		0.022 REF.	
$\theta$	0°	8°	0°	8°

## Notes

1. All dimensions are in millimeters.
2. Tolerance  $\pm 0.10\text{mm}$  (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.





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