

P-Channel Enhancement Mode MOSFET

GENERAL DESCRIPTION

The PW3407 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

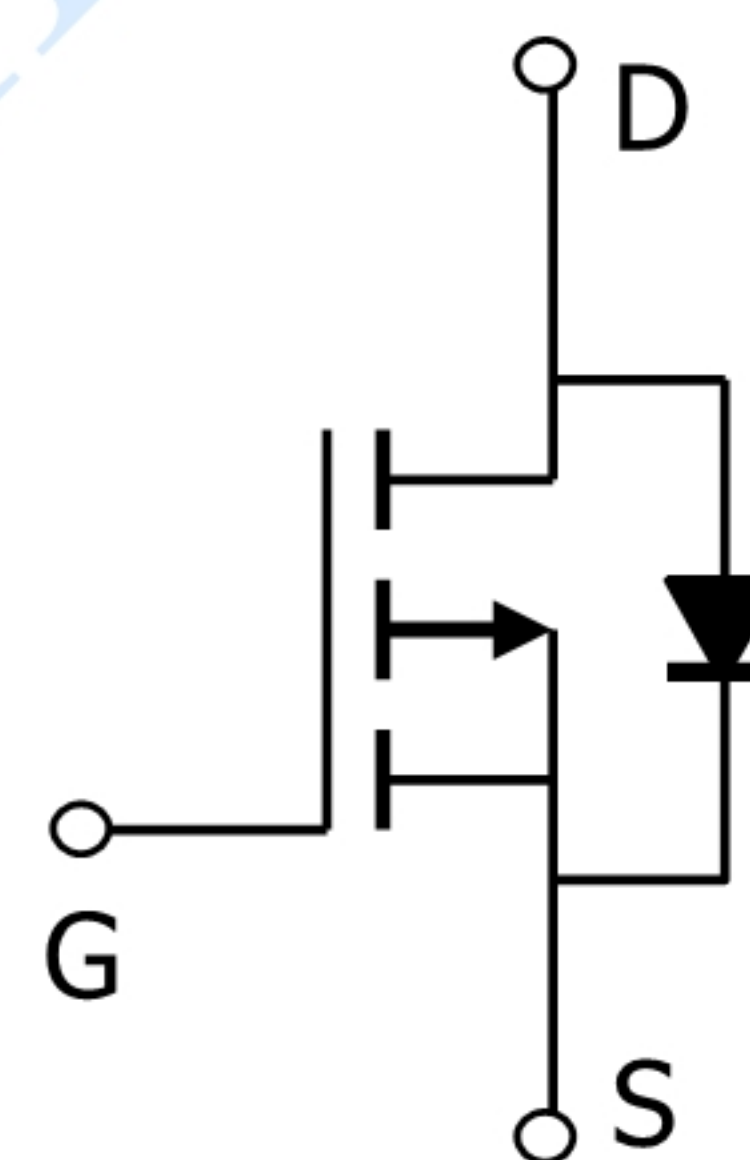
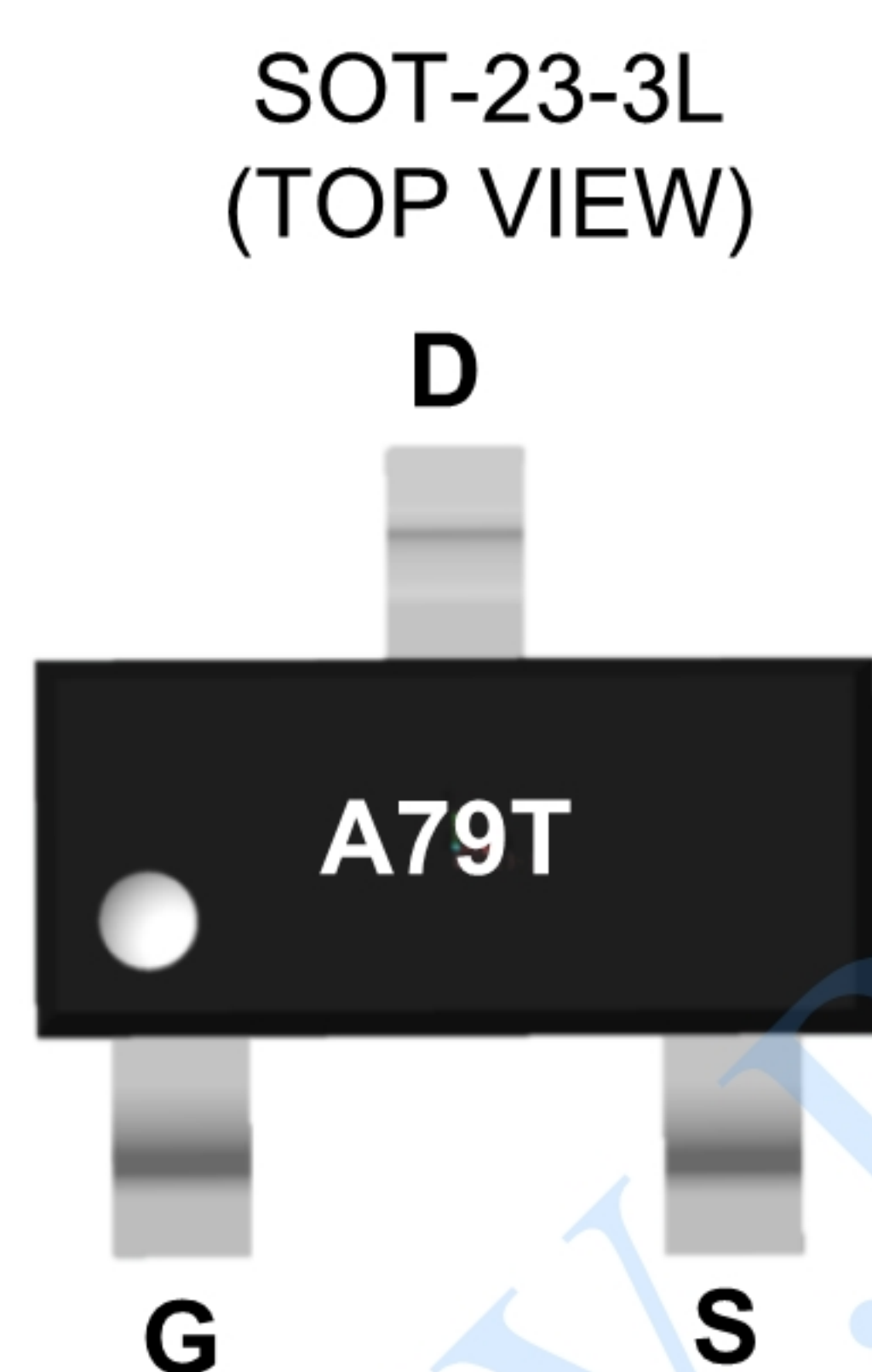
FEATURES

$V_{DS} = -30V, I_D = -4.2A$

$R_{DS(ON)} < 65m\Omega @ V_{GS} = -10V$

$R_{DS(ON)} < 90m\Omega @ V_{GS} = -4.5V$

Available in a 3-Pin SOT23-3 Package



Absolute Maximum Ratings (TA=25°C unless otherwise noted)

| Symbol | Parameter | Rating | Units |
|--------------------------|---|------------|--------------|
| V_{DS} | Drain-Source Voltage | -30 | V |
| V_{GS} | Gate-Source Voltage | ± 20 | V |
| $I_D @ T_A = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ -10V^1$ | -4.2 | A |
| $I_D @ T_A = 70^\circ C$ | Continuous Drain Current, $V_{GS} @ -10V^1$ | -3.1 | A |
| I_{DM} | Pulsed Drain Current ² | -17 | A |
| $P_D @ T_A = 25^\circ C$ | Total Power Dissipation ³ | 1.32 | W |
| $P_D @ T_A = 70^\circ C$ | Total Power Dissipation ³ | 0.84 | W |
| T_{STG} | Storage Temperature Range | -55 to 150 | $^\circ C$ |
| T_J | Operating Junction Temperature Range | -55 to 150 | $^\circ C$ |
| $R_{\theta JA}$ | Thermal Resistance Junction-Ambient ¹ | 125 | $^\circ C/W$ |
| $R_{\theta JA}$ | Thermal Resistance Junction-Ambient ¹ ($t \leq 10s$) | 95 | $^\circ C/W$ |
| $R_{\theta JC}$ | Thermal Resistance Junction-Case ¹ | 80 | $^\circ C/W$ |



ELECTRICAL CHARACTERISTICS

(TA = 25°C, unless otherwise noted.)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|------------------------|--|---|------|--------|------|-------|
| BVDSS | Drain-Source Breakdown Voltage | V _{GS} =0V, I _D =-250uA | -30 | -36 | --- | V |
| ΔBVDSS/ΔT _J | BV _{DSS} Temperature Coefficient | Reference to 25°C, I _D =-1mA | --- | -0.023 | --- | V/°C |
| RDS(ON) | Static Drain-Source On-Resistance ² | V _{GS} =-10V, I _D =-3A | --- | 50 | 65 | mΩ |
| | | V _{GS} =-4.5V, I _D =-2A | --- | 65 | 90 | |
| VGS(th) | Gate Threshold Voltage | V _{GS} =V _{DS} , I _D =-250uA | -1.2 | -1.6 | -2.5 | V |
| ΔVGS(th) | V _{GS(th)} Temperature Coefficient | | --- | 4 | --- | mV/°C |
| IDSS | Drain-Source Leakage Current | V _{DS} =-24V, V _{GS} =0V, T _J =25°C | --- | --- | -1 | uA |
| | | V _{DS} =-24V, V _{GS} =0V, T _J =55°C | --- | --- | -5 | |
| IGSS | Gate-Source Leakage Current | V _{GS} =±20V, V _{DS} =0V | --- | --- | ±100 | nA |
| gfs | Forward Transconductance | V _{DS} =-5V, I _D =-3A | --- | 11 | --- | S |
| Q _g | Total Gate Charge (-4.5V) | V _{DS} =-15V, V _{GS} =-4.5V, I _D =-3A | --- | 6.4 | 9.0 | nC |
| Q _{gs} | Gate-Source Charge | | --- | 2.3 | 3.2 | |
| Q _{gd} | Gate-Drain Charge | | --- | 1.9 | 2.7 | |
| Td(on) | Turn-On Delay Time | V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-3A | --- | 2.8 | 5.6 | ns |
| T _r | Rise Time | | --- | 8.4 | 15.1 | |
| Td(off) | Turn-Off Delay Time | | --- | 39 | 78.0 | |
| T _f | Fall Time | | --- | 6 | 12.0 | |
| C _{iss} | Input Capacitance | V _{DS} =-15V, V _{GS} =0V, f=1MHz | --- | 583 | 816 | pF |
| C _{oss} | Output Capacitance | | --- | 100 | 140 | |
| Crss | Reverse Transfer Capacitance | | --- | 80 | 112 | |
| I _S | Continuous Source Current ^{1,4} | V _G =V _D =0V, Force Current | --- | --- | -3.3 | A |
| ISM | Pulsed Source Current ^{2,4} | | --- | --- | -17 | A |
| VSD | Diode Forward Voltage ² | V _{GS} =0V, I _S =-1A, T _J =25°C | --- | --- | -1 | V |
| t _{rr} | Reverse Recovery Time | I _F =-3A, dI/dt=100A/μs, T _J =25°C | --- | 7.8 | --- | nS |
| Q _{rr} | Reverse Recovery Charge | | --- | 2.5 | --- | nC |

Note : .

- 1、 The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、 The power dissipation is limited by 150°C junction temperature
- 4、 The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

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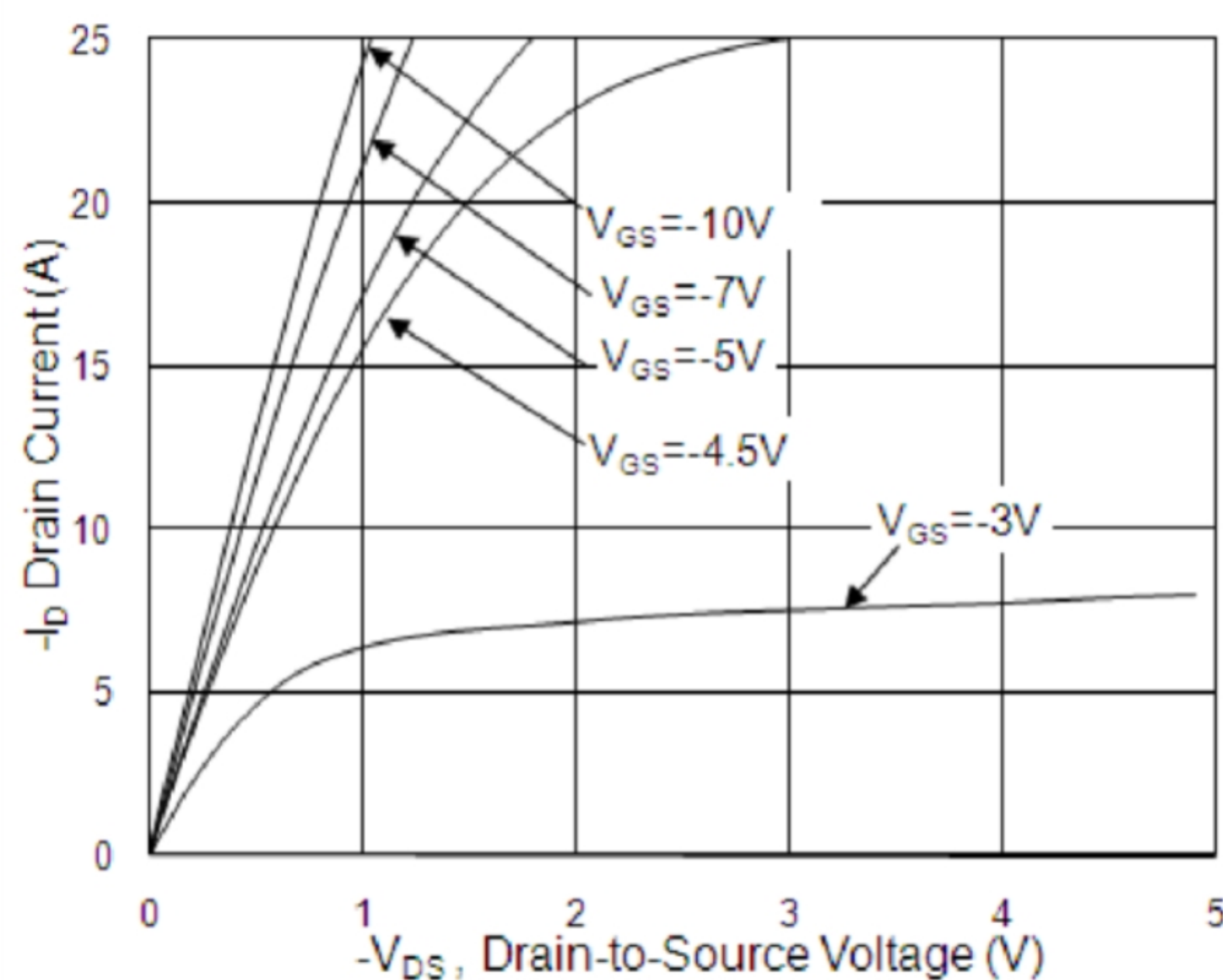


Fig.1 Typical Output Characteristics

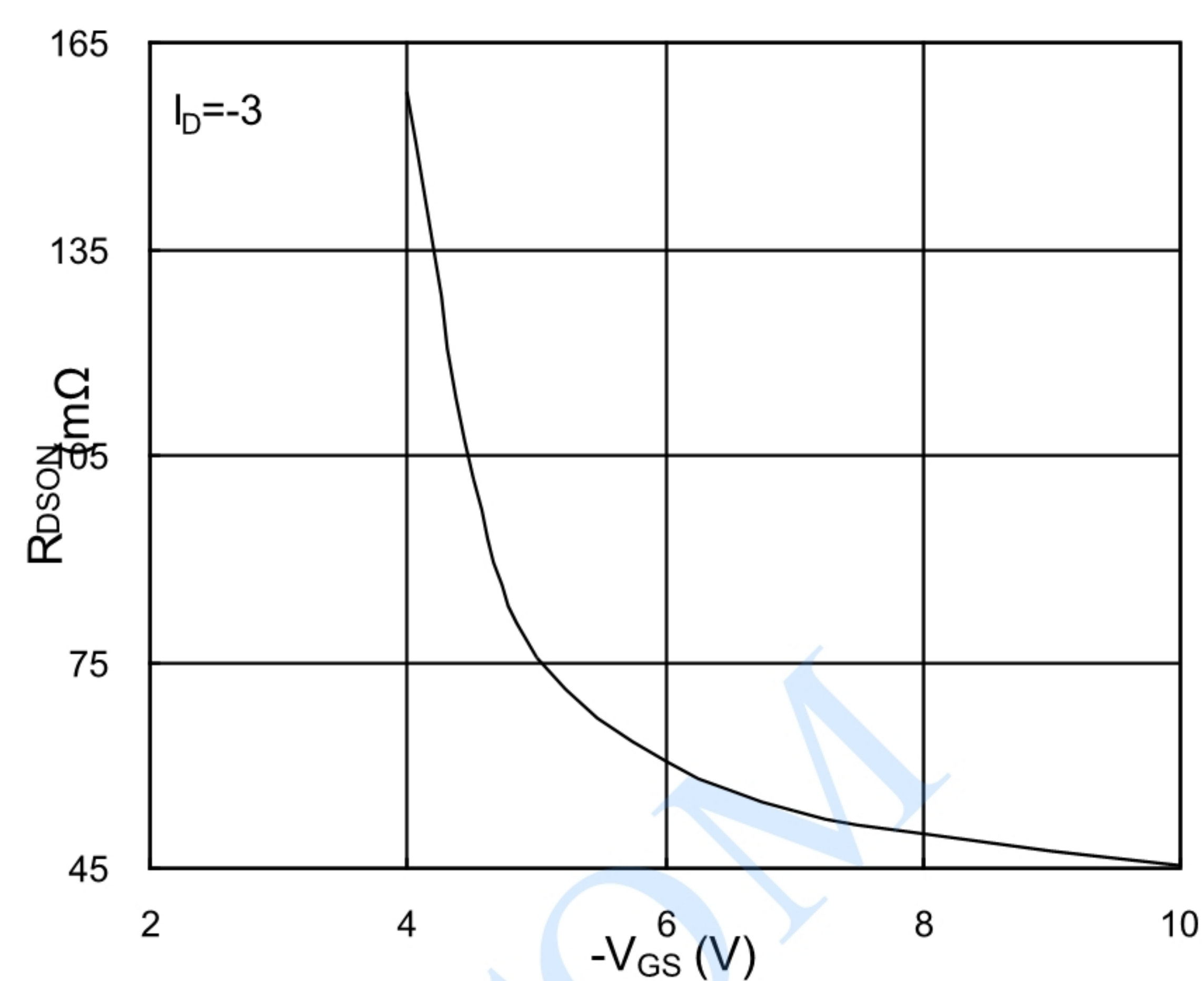


Fig.2 On-Resistance v.s Gate-Source

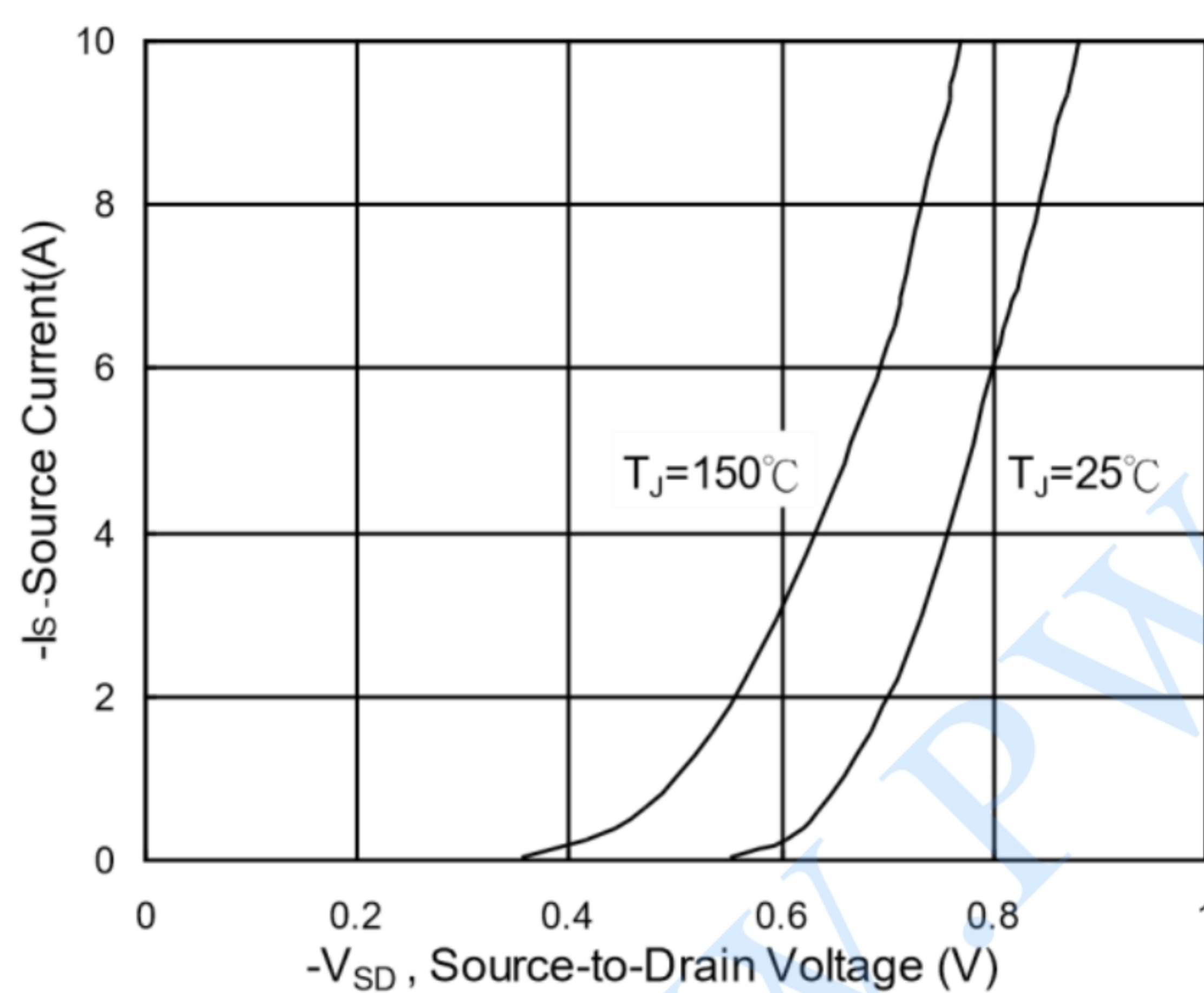


Fig.3 Forward Characteristics of Reverse

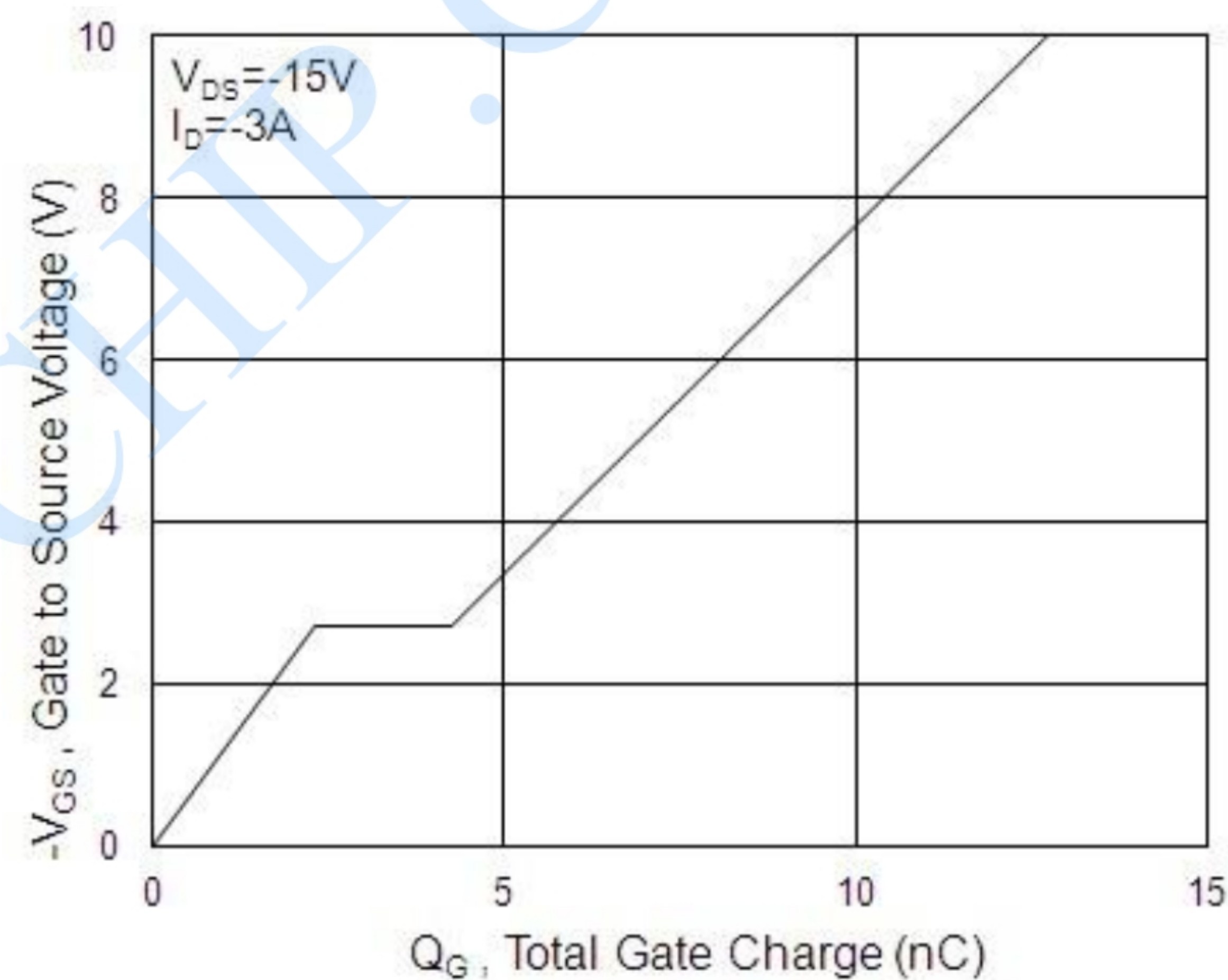


Fig.4 Gate-Charge Characteristics

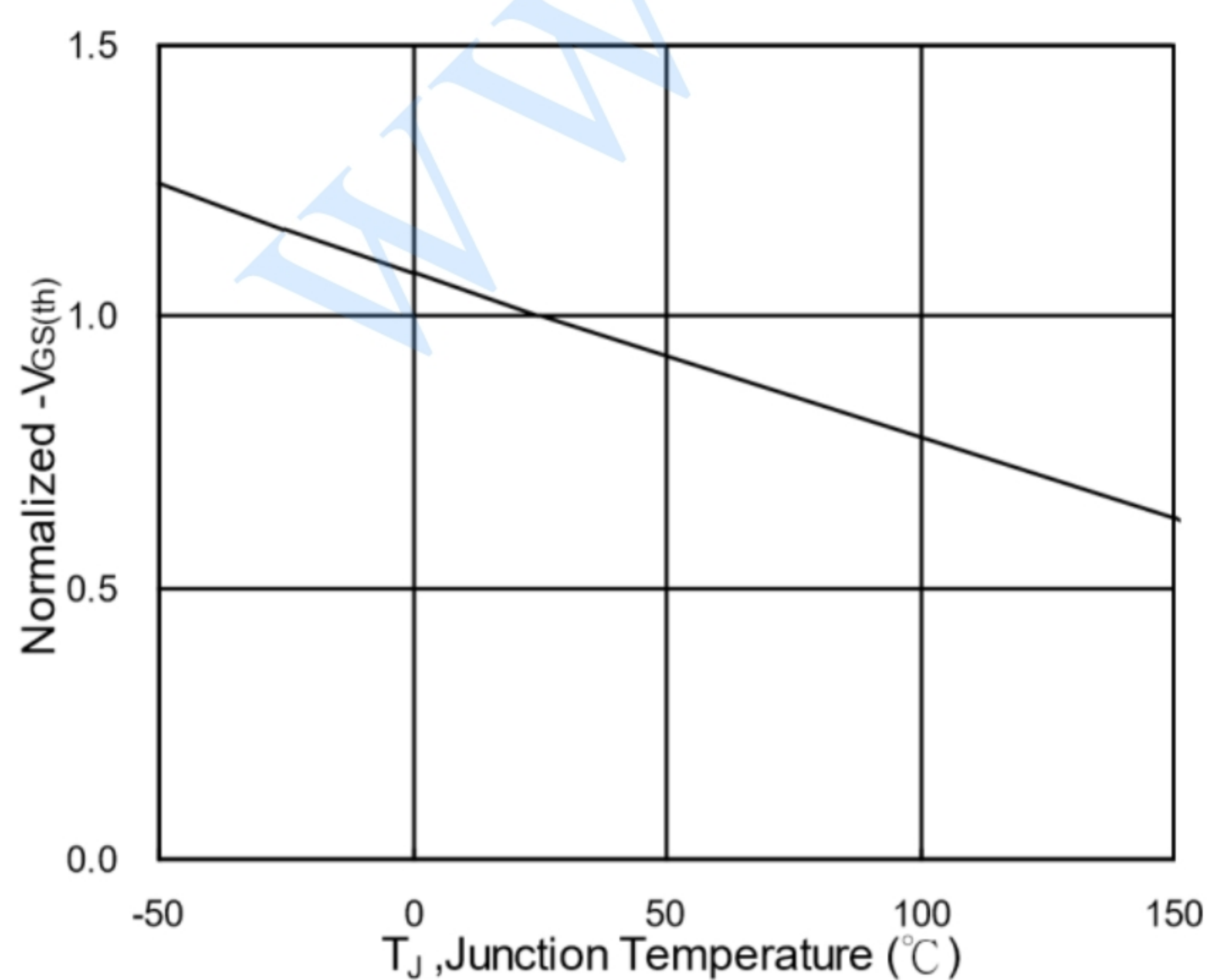


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

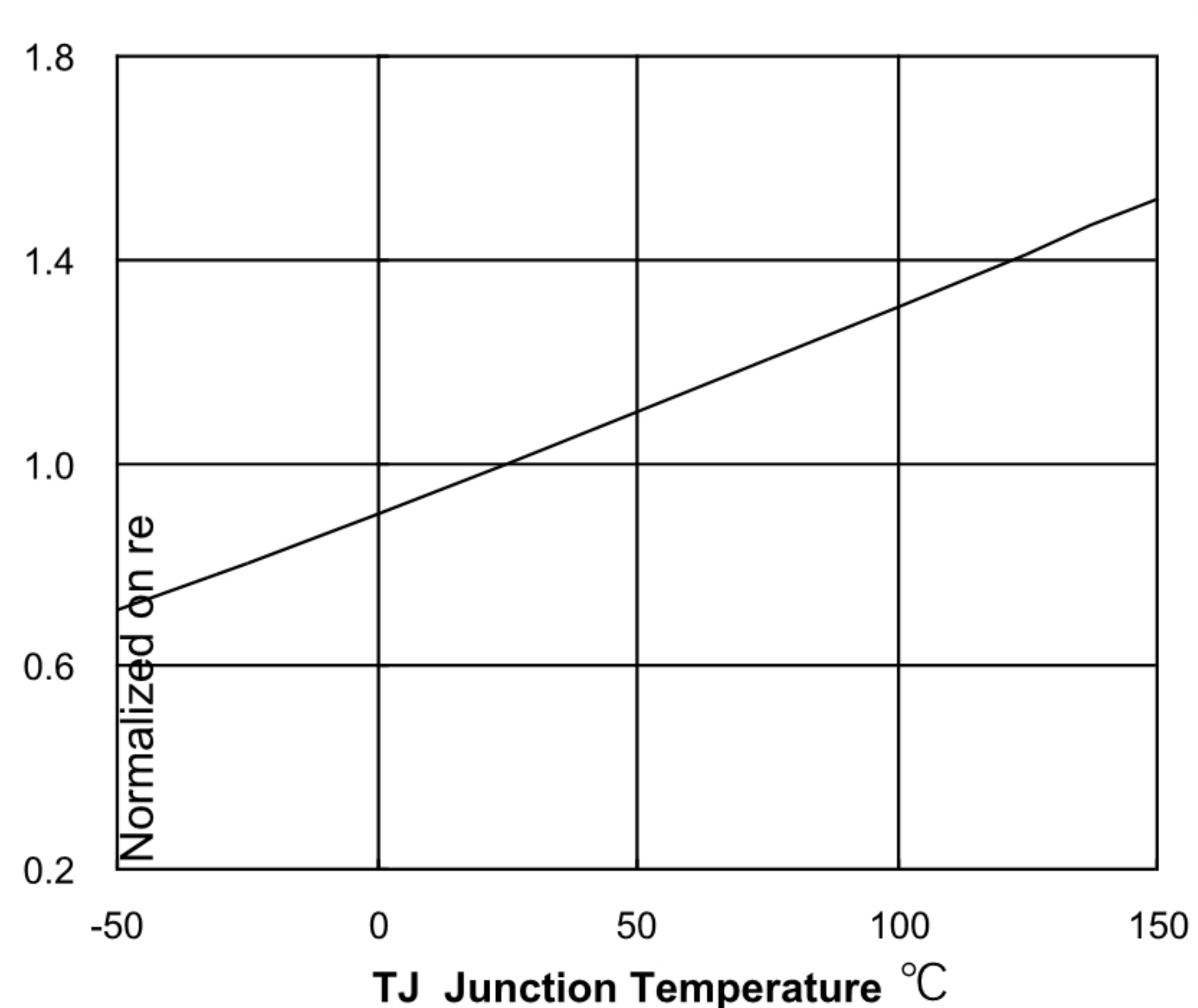


Fig.6 Normalized $R_{DS(on)}$ vs T_J

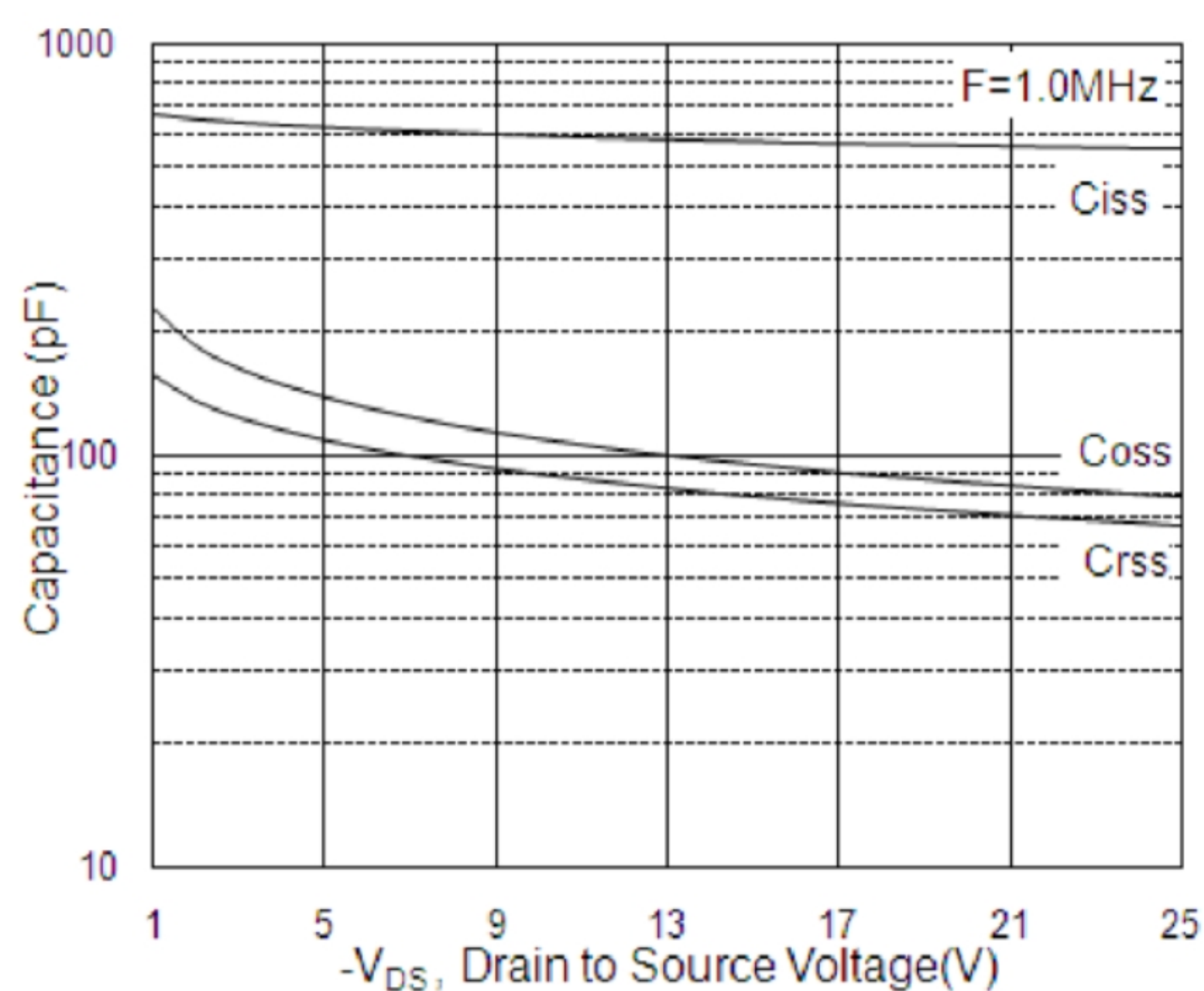


Fig.7 Capacitance

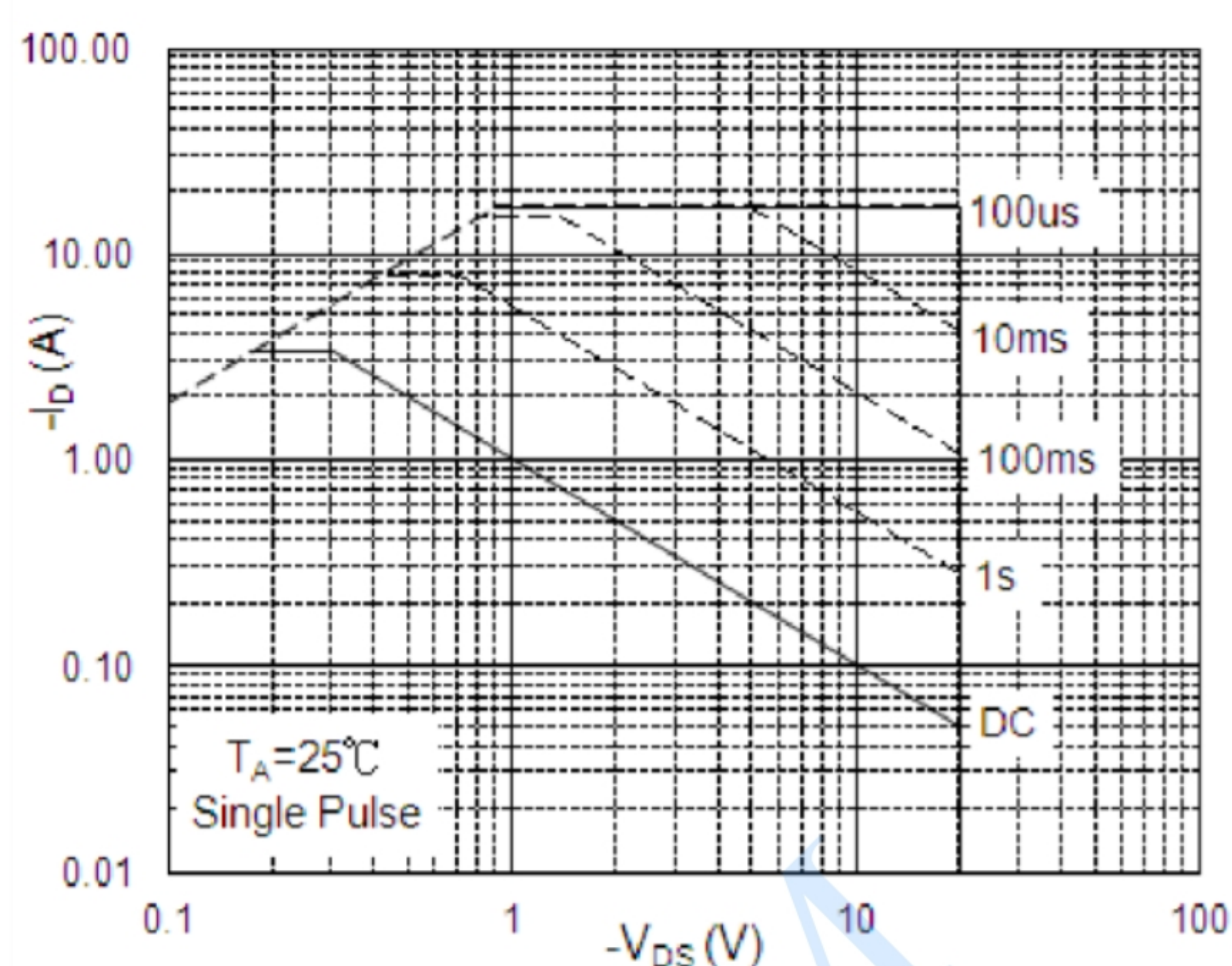


Fig.8 Safe Operating Area

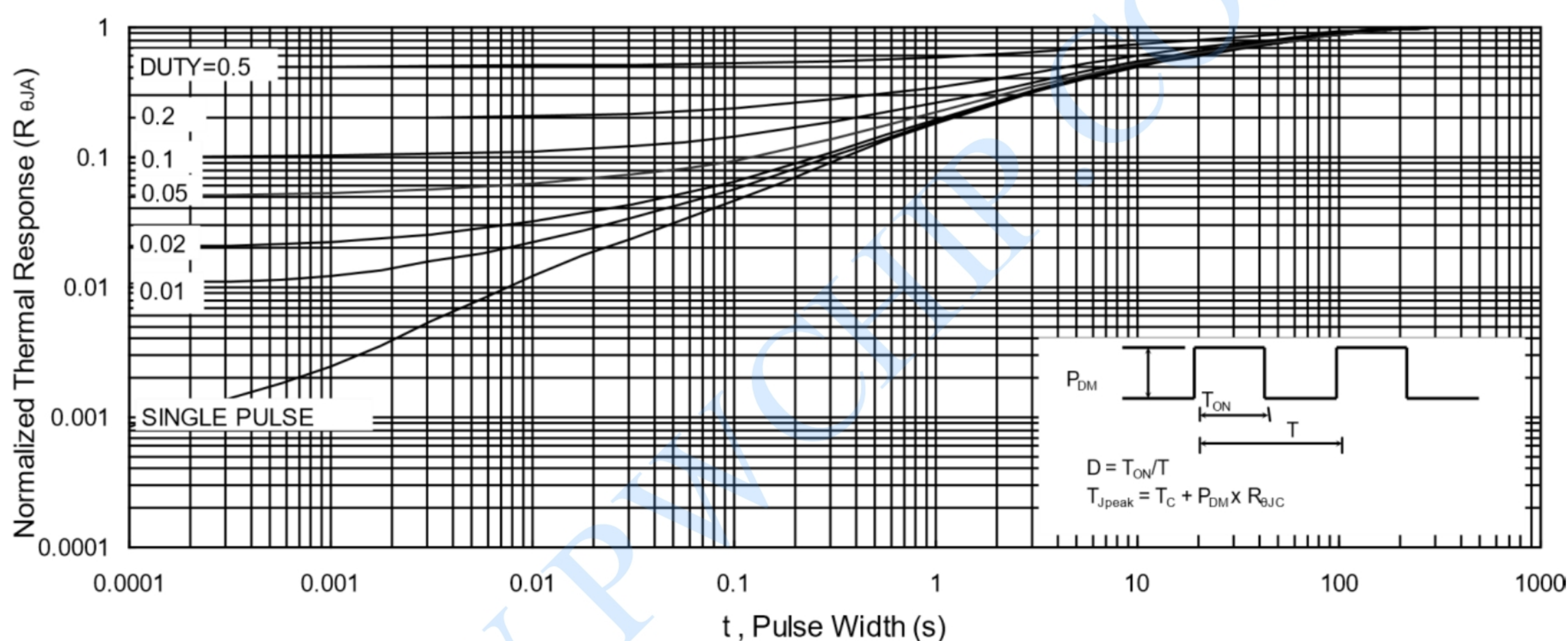


Fig.9 Normalized Maximum Transient Thermal Impedance

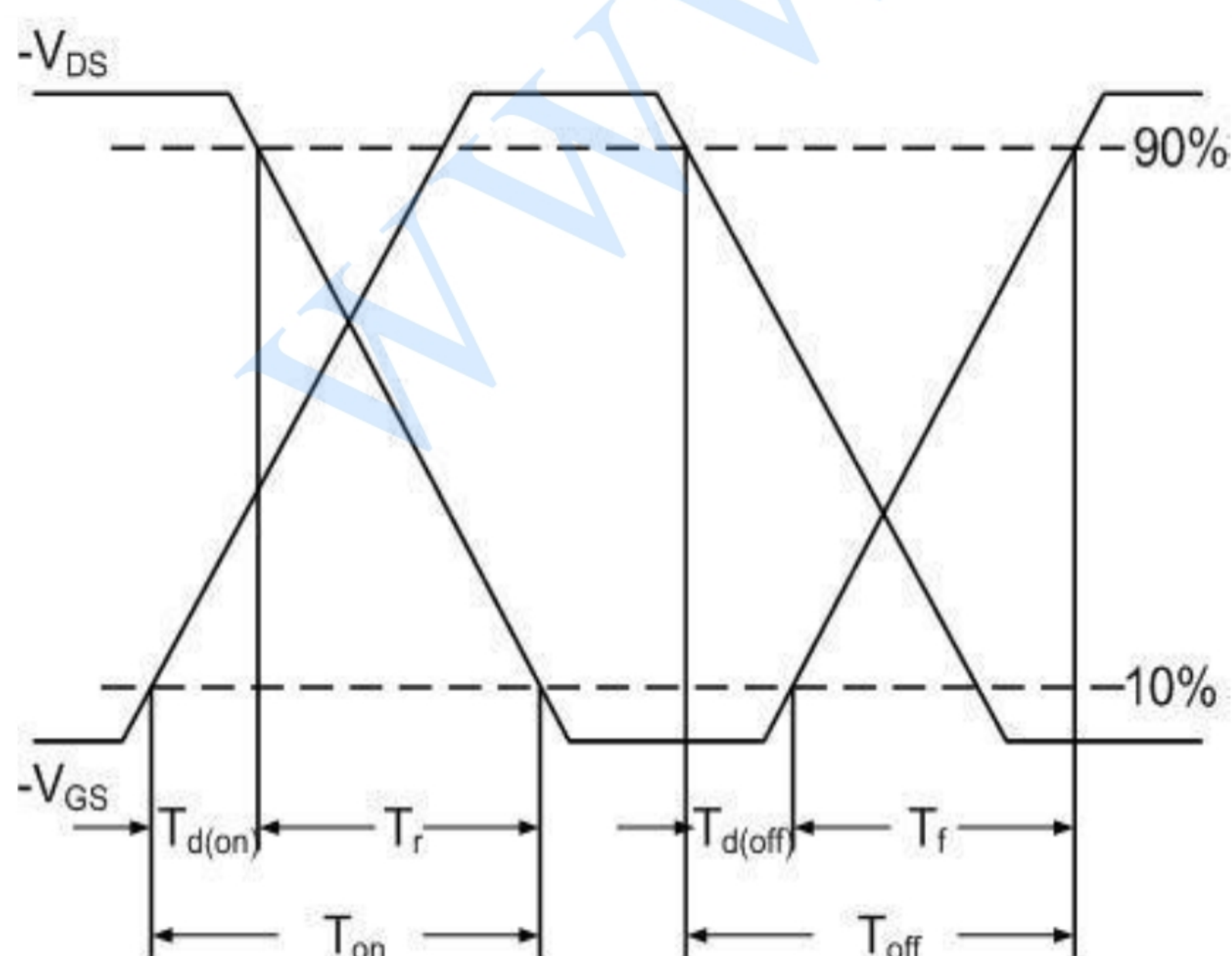


Fig.10 Switching Time Waveform

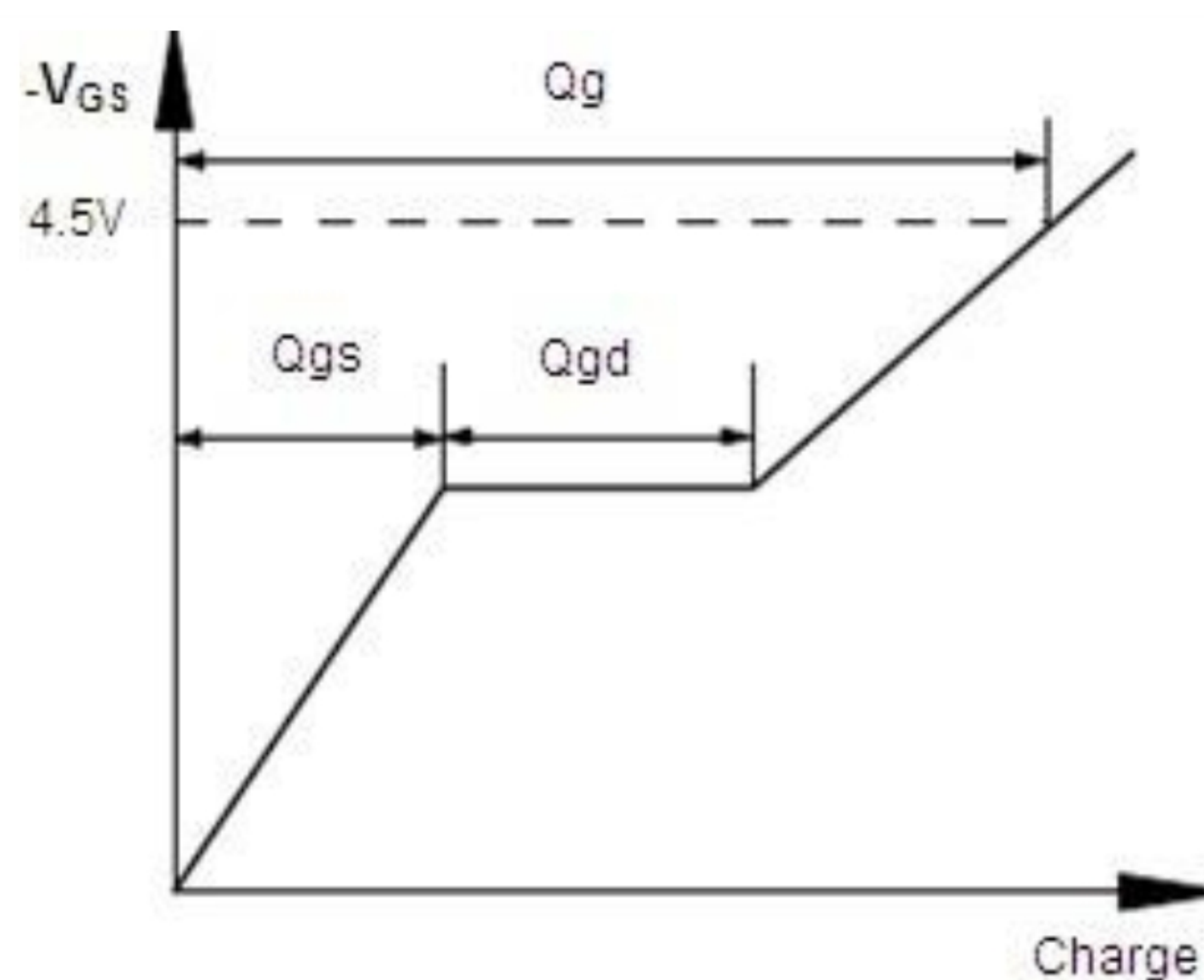
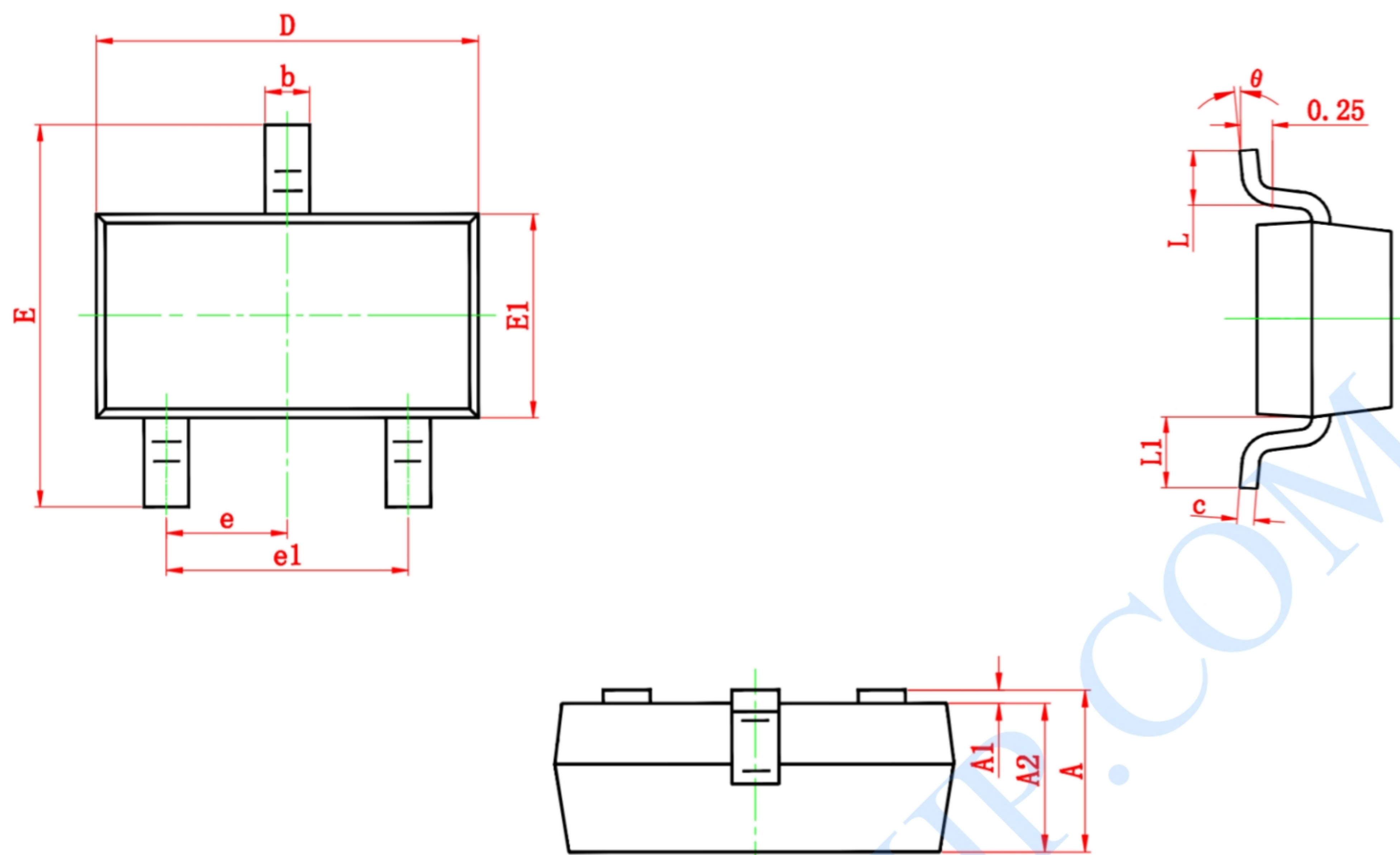


Fig.11 Gate Charge Waveform

PACKAGE DESCRIPTION

SOT23-3



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min. | Max. | Min. | Max. |
| A | 0.900 | 1.150 | 0.035 | 0.045 |
| A1 | 0.000 | 0.100 | 0.000 | 0.004 |
| A2 | 0.900 | 1.050 | 0.035 | 0.041 |
| b | 0.300 | 0.500 | 0.012 | 0.020 |
| c | 0.080 | 0.150 | 0.003 | 0.006 |
| D | 2.800 | 3.000 | 0.110 | 0.118 |
| E | 2.250 | 2.550 | 0.089 | 0.100 |
| E1 | 1.200 | 1.400 | 0.047 | 0.055 |
| e | 0.950 TYP. | | 0.037 TYP. | |
| e1 | 1.800 | 2.000 | 0.071 | 0.079 |
| L | 0.300 | 0.500 | 0.012 | 0.020 |
| L1 | 0.550 REF. | | 0.022 REF. | |
| θ | 0° | 8° | 0° | 8° |

Notes

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.



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